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EETIMES

The industry newsweekly for the creators of technology

ISSUE 1376

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MONDAY, JUNE 20, 2005

Mr. Moonshot

Cognitive radios are our future, but only “moon-shot” research and development will get us there. Jeff Reed explains why and how in this week’s Interview on page 24.



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Media Access Gateway	●					
IP PBX	●	●				
Gateways & IADs	●	●				
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Wireless Transcoding	●					
Video Transcoding	●					
Terminal Adaptor		●				●
Switch/Router						●
Home Gateway			▲			
Triple Play						
V2IP Phone/TV Out			▲	▲▲		
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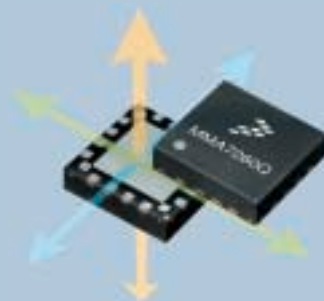
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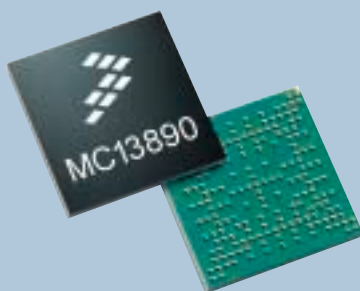
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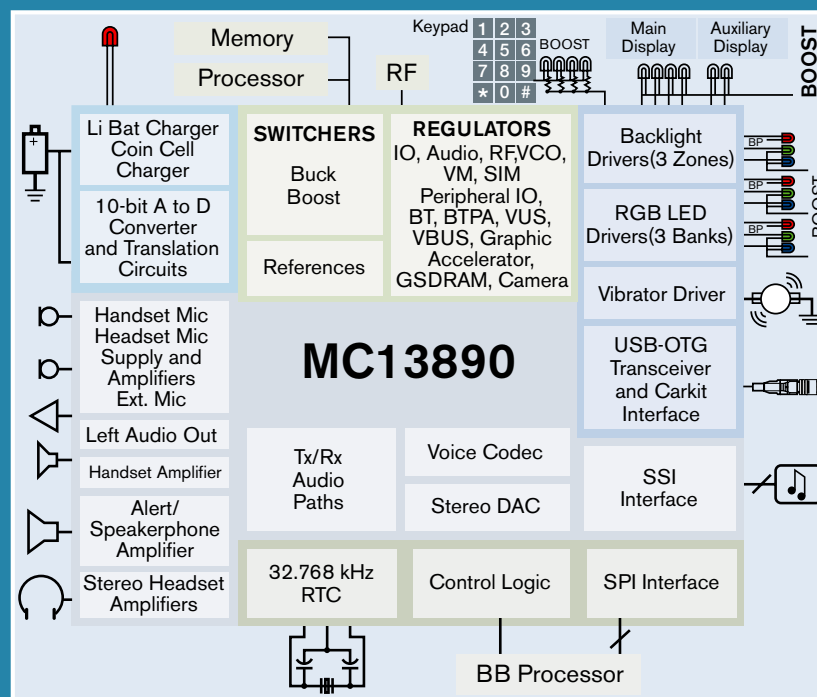
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ISSUE 1376

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MONDAY, JUNE 20, 2005

Millions of dollars	2003	2004	% change
China	\$1,156	\$2,683	132.1%
Europe	\$2,558	\$3,444	34.6%
Japan	\$5,555	\$8,276	49.0%
Korea	\$3,176	\$4,614	45.2%
North America	\$4,728	\$5,812	22.9%
Taiwan	\$2,917	\$7,762	166.1%
Rest of world	\$2,097	\$4,490	114.1%
Total regions	\$22,189	\$37,081	67.1%

Source: SEMI-STAT

Taiwan was the only semiconductor equipment market to outstrip China in year-on-year growth in 2004.

China gets its head into gear

By Mike Clendenin and Mark LaPetus

Shanghai, China — China is putting down roots for a domestic semiconductor and materials industry that could eventually go global, posing a potential threat to competitors and intellectual-property protections.

No one thinks this will take place overnight, but many consider it inevitable. As part of China's wider strategy of self-reliance, building a semiconductor equipment and materials industry would allow Chinese companies to glean more benefit from the country's fast-growing semiconductor and electronics market.

China already has several local wafer suppliers, which mostly serve the country's 4-, 5-

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Tools missing as ESL rolls

Users seek support as design abstraction goes mainstream

By Richard Goering

Anaheim, Calif. — Soo-Kwan Eo had disconcerting news last week for anyone who's counting on electronic system-level design to be the catalyst for returning the EDA industry to growth. Eo, senior vice president at Samsung Electronics Co. Ltd., said that while Samsung's ESL resource allocation is increasing, its expenditure on commercial ESL tools is declining.

"We couldn't find the right tools," Eo said during a panel discussion here at the 42nd Design Automation Conference. So Samsung is working with universities and research institutes to develop its own, he said.

ESL appears at last to be making good on its promise—first proffered 10 years ago—to bring designers above the register-transfer level. Eo was one of several ESL users who reported at DAC that chip designers are starting to use system-level methodologies, particularly transaction-level modeling based on SystemC.

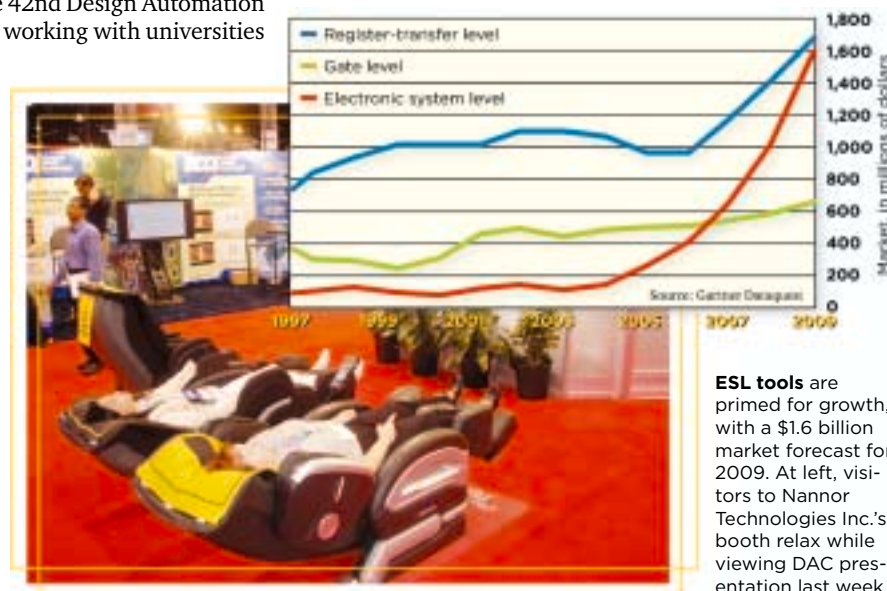
But that doesn't directly translate into EDA sales. While some designers reported using com-

mercial ESL tools, others are rolling their own or are using open-source software available from Open SystemC International (OSCI). And all came to DAC with wish lists of capabilities that commercial tools have yet to meet.

The ESL field should provide plenty of opportunity. At the annual Gartner Dataquest briefing at DAC, chief analyst Daya Nadamuni predicted a surge in ESL revenues, from about \$200 million today to \$1.6 billion in 2009. At that point, ESL and RTL tool revenues would be roughly equivalent. "What will it take to drive [EDA] growth to double digits?" she asked. "It really seems like ESL is going to be the savior."

At the same briefing, however, Gartner Dataquest Inc.

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Beyond the Horizon



By Loring Wirbel

Warren Ryd and Barbara Doyle almost resorted to constructing a makeshift microwave tower last month in the backyard of their Black Forest, Colo., home. The couple isn't particularly consumed with microwave links; they're not even RF-savvy. They're two people trying to build an Internet consulting business.

That's easier said than done in Black Forest. The town lies a few short miles from the sprawling, ultramodern exurbs on the eastern fringes of Colorado Springs and is just 22,000 feet from the nearest Qwest Communications central office. But for the area's incumbent phone and cable operators, Black Forest, Colo., might just as well be Germany's

Black Forest—simply too remote to care about.

An undercapitalized Qwest has struggled to continue digital-subscriber-line buildouts in its vast but sparsely populated service area. And Adelphia Communications' struggles with bankruptcy and a corporate selloff mean that a hybrid fiber-coax plant

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> DAC captured

EE Times interviewed a variety of people—industry analysts, company presidents, marketers and press agents—for their impressions of the Design Automation Conference. See what the video camera captured at eetimes.com



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the week in review

IDT moves to expand

In a major move to expand its product offerings, **Integrated Device Technology Inc.** (IDT) announced plans last week to acquire **Integrated Circuit Systems Inc.** for \$1.7 billion. The chip makers said the deal will provide a platform for growth in the communications, computing and consumer markets. For the 12 months ended March 31, the combined company had revenue of about \$645 million and generated \$86 million in cash flow. The new company will retain the IDT name and have headquarters in San Jose, Calif.

Chip index rises

North American-based manufacturers of semiconductor equipment posted a book-to-bill ratio of 0.85 in May, an increase from 0.81 in April, according to the **Semiconductor Equipment and Materials International** (SEMI) trade group. A book-to-bill of 0.85 means that the manufacturers received \$85 worth of orders for every \$100 of product billed for the month. The SEMI book-to-bill is a ratio of three-month moving averages of the worldwide bookings and billings for North American-based semiconductor equipment manufacturers.

EET's Goering feted

Richard Goering, *EE Times*' veteran EDA editor, was honored at last week's Design Automation Conference (DAC) for authoritative coverage of the EDA industry over the past 20 years. Goering, editorial direc-



EE Times'
Goering:
20 years
on the
EDA beat.

tor for design automation, was the first technology journalist to be honored by the group. "Richard's contributions to the furtherance of knowledge and the evolution of design automation have been invaluable," said Bill Joyner, DAC general chairman. Goering, a longtime panel moderator at DAC, joined *EE Times*' parent company, **CMP Media LLC**, in 1989 and has directed EDA coverage since 1990. He previously reported on the industry for *Computer Design* magazine and a Silicon Valley publication.

Computer hiring up

The hiring of computer scientists increased sharply in the first quarter, according to U.S. statistics compiled by **IEEE-USA**. Figures released by the Labor Department's Bureau of Labor Statistics showed an increase of 54,000 jobs in computer science and systems analysis, which was a jump of 7.7 percent over the 2004 average.

DRAM cell scaled

Sony Corp. and **Toshiba Corp.** say they have developed the first 45-nanometer embedded DRAM cell made by scaling embedded DRAM cells down to 0.069 square micron. The companies' findings were reported in a paper at the 2005 VLSI Symposium in Kyoto, Japan. Sony and Toshiba said they jointly developed 90- and 65-nm process technologies, which Toshiba calls CMOS4 and CMOS5, respectively. They will next collaborate on development of 45-nm process technology.

Correction

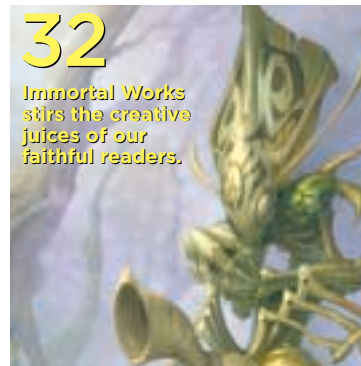
A June 13 story about the **Albany Nanotech** research center misstated funding levels and sources. The center has received \$500 million in funding commitments from the State of New York, and \$2.4 billion in funding commitments from industry.

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June 20, 2005

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Immortal Works stirs the creative juices of our faithful readers.



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Opinion

Contrary to the Defense Science Board's report, changes in the U.S. IT industry won't lead to its demise

Globalization? Bring it on

In the past few years, there has been no shortage of reports and rhetoric bemoaning the apparent downward spiral of America's dominance in IT. The latest declaration that the sky is falling comes from an adviser to the Defense Department, in what may be one of the starkest descriptions of the downside implications of globalization in the chip and electronics industries.

The authors of the Defense Science Board's report on high-performance microchip supply believe globalization of the industry is a clear and present danger to U.S. national security. "The potential effects of this restructuring are so perverse and far-

reaching and have such opportunities for mischief that, had the United States not significantly contributed to this migration, it would have been considered a major triumph of an adversary nation's strategy to undermine U.S. military capabilities," the authors write.

That's strong stuff. There's more, too—a lot more. In 118 pages, the authors hopscotch through a multiplicity of issues: fewer fabs being built in the United States, spiraling ASIC costs, stalled R&D funding, the sale of advanced semiconductor manufacturing equipment to potential rivals (China) and concern over the U.S. work force's long-term competitiveness.

Even a casual glance at the issues prompts readers to connect the dots to form a grim picture: America's technical prowess is seriously at risk.

Maybe it is, at least from the narrow perspective of the Defense Department. It needs "trusted" sources of semiconductors and electronic components, along with a competitive U.S.-based infrastructure that leads to reasonable prices. Undoubtedly, production facilities available to the DOD are diminishing in the United States, with IBM remaining as one of its main sources for ASICs.

The conclusions in the report are sobering. Moreover, they are indicative of a new order. Emerging markets like China are becoming major sources of revenue for companies like Intel, Nokia, Motorola and Texas Instruments, and the talent in China and India will help U.S. and European companies expand on their success. Naturally, the aforementioned companies will also be investing in those places.

With Asia being the driver of growth for probably the next 50 to 100 years, it seems unreasonable for the United States to maintain its dominance, particularly in IC manufacturing. Instead, it will likely share leadership with other countries, some of which will surpass it

By Mike Clendenin, Taipei bureau chief

in certain areas, just like Japan and the Netherlands do in lithography equipment and Taiwan does in the foundry industry.

A major flaw of the Defense Science Board's report is that it harbors some hope that the U.S. IC industry can return to the days when much of the design and production was U.S.-based. The Semiconductor Industry Association seems to share this hope. It has argued that more favorable tax policies are needed to attract fab investment to the United States and away from Asia—especially China. In April, SIA president George Scalise told the U.S.-China Economic and Security Review Commission that about two-thirds of the 300-mm wafer fabrication facilities being built are in Asia, "with a significant portion of those facilities in China." He went on to argue

that "Chinese government policies—not lower labor costs—are the principal factor" in drawing those fabs to China.

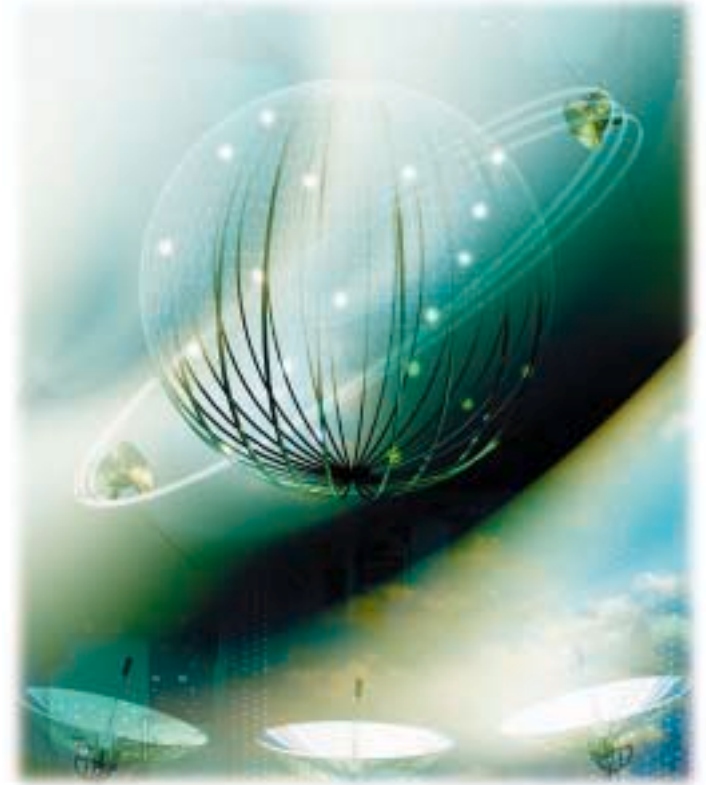
In reality, China has only one 300-mm wafer fab, in Beijing. One, period. So the sky is not falling. More important, there are other measures of U.S. competitiveness. For instance, it is still a top destination for engineers and students

(those who can get visas), and Silicon Valley is still considered the mecca of the IT world, with companies that consistently rank tops among patent winners. The United States also dominates the fabless design industry.

Giving the likes of Intel more tax breaks to keep fabs in the United States is probably untenable policy, since the government would have to almost match the "tax holidays" of China and Taiwan, which would do little to affect the U.S. IC industry's long-term health. Indeed, Taiwan is considering tax reform that would install a minimum alternative tax because the industry here has not paid its fair share of the tax burden since maturity.

Rather, Intel's Craig Barrett had it right when he called for long-term spending increases in basic R&D.

We can't match Asia's tax breaks. Our best defense is more funding for basic R&D.



For if America's tech industry truly is in decline (certainly arguable), then that will help arrest the fall. Engineers can help themselves by being active in organizations that espouse greater funding for university and industry R&D, or greater funding for federal education mandates. They can also continually add new skill sets, whether in engineering or in second languages.

Asia will continue to grow into its potential. That is an immutable fact, and a good one. "It will be the best thing that happened to the West, because it will challenge us," said venture capitalist Joseph Schoendorf in an April address in Beijing. "Remember what happened in Silicon Valley in the mid-'70s? We raised our hands in surrender [to Japan]. The U.S. is dead, we said. . . . And [Intel's] Andy Grove threw in the towel and said, 'We're out of the DRAM business. But we have an idea for a thing called a microprocessor.' And it changed the world."

Sometimes, the grinding competition from Asia will be untenable, because of its low-cost structure. But that will force the United States, and Europe, toward greater innovation. Meanwhile, in Asia (except for Japan), innovation is still hindered in many areas by a lack of true knowledge ownership.

The sole dissenting voice in the recent report for the Defense Department, Thomas Hartwick, noted that innovation and leadership will be the key that America's tech industry needs to stay ahead.

"To be more blunt," Hartwick said, "it is not DOD's job to revamp the infrastructure of this healthy, robust and very profitable industry. . . . Our nation would be better served if government provided the catalyst or leadership (nonfinancial support), apparently missing in the semiconductor industry, to facilitate a better semiconductor industry long-term strategic plan."

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News

IBM, defending supercomputer crown, eyes NEC

By R. Colin Johnson

Portland, Ore. — NEC could be bidding to reclaim its place as maker of the world's fastest supercomputer when unofficial rankings are announced this week. But IBM, which toppled NEC from that perch a year ago, plans to defend its crown and last week added a world-class contender to the field.

Indeed, until the latest challenge from NEC, it appeared likely that IBM would take three of the top five positions in the new ranking of supercomputers and that another U.S. company, Silicon Graphics, would nail down a fourth.

The list is to be released at the 20th International Supercomputer Conference, which begins tomorrow in Heidelberg, Germany.

IBM Corp. (Armonk, N.Y.) expected to snag the top two slots. Silicon Graphics Inc. (Mountain View, Calif.) and Tokyo-based NEC Corp. were expected to vie for third and fourth, with IBM also taking the fifth spot. Prestigious supercomputing systems are seen as a measure of scientific and national competitiveness.

In the early betting, IBM's BlueGene/L supercomputer was the odds-on favorite to retain the top slot with 91.8-teraflops peak performance. The BlueGene/L uses 32,768 PowerPC440 central processing units and is being upgraded to 130,000 CPUs, to yield a projected performance of 360 Tflops. The BlueGene/L is installed at the U.S. Department of Energy's Lawrence Livermore National Laboratory (Livermore, Calif.).

Moving into second place was an IBM supercomputer dubbed BlueGene/W, recently installed at IBM's Thomas J. Watson Research Center in Yorktown Heights, N.Y., and billed last week as the world's most powerful privately owned supercomputer. The BlueGene/W tops 91.29 Tflops using more than 30,000 PowerPC CPUs.

Third place was expected to go to Silicon Graphics' Altix system, housing 10,160 Voltaire Infiniband 1.5-GHz CPUs and topping 60.9 Tflops. The system is installed at the National Aeronautics and



Big Blue is banking on its BlueGenes to snag the top two slots in the world supercomputer standings.

Space Administration's Ames Research Center in Mountain View, Calif.

Fourth place was expected to go to NEC's Earth Simulator, which uses 5,120 CPUs to top 40.9 Tflops in its SX-6 spin. But an updated model, the SX-8, is said to have three times the horsepower of its predecessor and could, if it lives up to its billing, mean all bets are off in the supercomputer standings.

If the NEC challenge does not material-

ize, IBM's Barcelona Supercomputer Center in Spain is expected to nail down fifth place. It has 3,564 PowerPC970 CPUs running at 2.2 GHz, which enables it to best 31.4 Tflops.

The fastest supercomputer list will be released by the "Top500" organization (<http://top500.org>), which independently assesses supercomputer performance.

Its latest list was released last November. Top500 measures supercomputer performance using the "Linpack" benchmark. Linpack was created by University of Tennessee computer science professor Jack Dongarra to compare computers that are solving a dense system of linear equations.

The Top500 version permits the supercomputer owner to scale the size of the problem and to optimize it to achieve both a best peak and sustained performance metric. While not reflecting the overall performance of a supercomputer, Linpack is widely accepted as a measure of peak performance of large multiprocessor computer systems.

CMOS takes a stab at deflating GaAs' RF dominance

By Stephan Ohr

San Francisco — Is gallium arsenide losing its hegemony among designers of RF modules? The threat from RF CMOS and BiCMOS with silicon germanium implants was a lively topic of conversation at the MTT-S 2005 International Microwave Symposium in Long Beach, Calif., last week.

Many participants in a panel session agreed that RF CMOS may be useful for low-cost, short-distance applications like WLANs and Bluetooth transceivers, but not for cell phone power amplifiers (PAs). GaAs will continue to dominate in that slot, some suggested.

Roughly 664.5 million cell phones shipped in 2004. At two or three power amps per phone, the total approached 2 billion PAs last year alone, said panel organizer Fazal Ali, manager of RF engineering and technology at phone maker Nokia. How many of those PAs were CMOS? "Not very many."

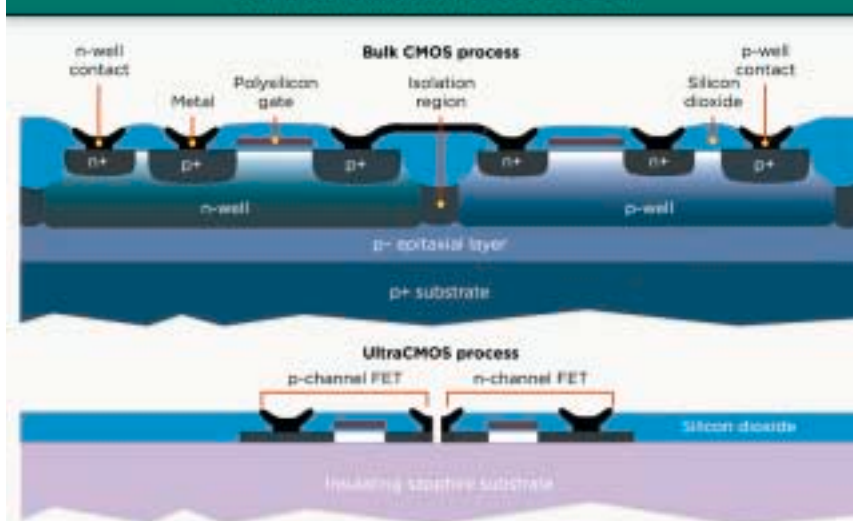
Co-organizer and moderator Mike Golio of HVVi Inc. (Phoenix) pondered the potential for displacing GaAs in cell phone PAs. Might CMOS PAs eventually dominate the mobile space? Would they coexist with III-V compound semiconductor processes or silicon bipolar junction transistors? Or would they remain the plaything of some adventurous designers, never capturing much market share?

CMOS has had no commercial successes in the handset PA market, said panelist Aditya Gupta, vice president of technology for GaAs transistor maker Anadigics Inc. Gupta's sentiments were echoed by Pete Zampard of Skyworks Solutions Inc. (Woburn, Mass.), which builds modules with both GaAs and silicon discretes.

CMOS, Zampard quipped, "stands for 'can't meet our specs.'"

Simpler process, higher performance

Transistor bandwidth reaches 100 GHz



Source: Peregrine Semiconductor Corp.

But Ali Hajimari, a professor of electrical engineering at the California Institute of Technology and co-founder of Axiom Microdevices Inc. (Orange, Calif.), said CMOS will be a formidable opponent for III-V PAs. Axiom has successfully demonstrated a single-chip, fully integrated quadband PA for GSM/GPRS applications in 0.13-micron CMOS, he claimed.

Hajimari cited 55 percent efficiency for the PA, a level that he believes is comparable to GaAs specs. The part includes matching I/Os and meets cellular designers' concerns for performance and ruggedness. The use of integrated CMOS PAs will pave the way for entire radios on the same chip, he said.

It is nonetheless likely that GaAs, RF CMOS and BiCMOS will coexist in many systems, panelists said.

"We are not striving to build an SoC [system-on-chip]," Rik Jos, a fellow in RF device technology for Philips Semiconductors (Nijmegen, Netherlands), told *EE Times*. The problem for integration, he said, is in building radios that operate on multiple frequencies and embody multiple standards. "Every generation will need a new PA, and there are only limited windows for accomplishing this on a CMOS SoC," Jos said.

Rather, Philips is building multichip modules for performance-oriented RF applications. "We integrate system-in-package, with the best or cheapest technology for each component," Jos said.

Like an express train

The persistent use of GaAs in RF designs, however, hasn't stopped manufacturers from pushing performance thresholds with CMOS devices. Peregrine Semiconductor Corp. (San Diego) has tweaked CMOS for use as an antenna switch and as a power amplifier, said

Rodd Novak, vice president of marketing.

Peregrine's Ultra CMOS process uses dielectric isolation, ensuring the performance of each MOS device in a complementary pair by isolating it from cross-coupling effects of the substrate. The technology is effectively silicon-on-insulator. Peregrine claims its 0.13-micron Ultra CMOS devices are less complicated to manufacture than GaAs and perform better than others' 90-nm CMOS at extended frequencies.

"Module design using GaAs transistors has been the traditional sweet spot for engineers," acknowledged Ted Miracco, vice president of Applied Wave Research Inc., an RF EDA tool maker. "But people are finding clever ways to do things in CMOS. We see that as the future—coming at us like an express train."



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News

Little time, big decisions for 45-nm node

By David Lammers

Kyoto, Japan — Technologists face some tough decisions in the coming weeks and months as they ponder which knobs to turn for the 45-nanometer node. With gains from gate oxide scaling and shorter channel lengths at a near standstill, process engineers are looking to a much different list of “boosters,” including further pushing strain in the silicon channels and high-k dielectrics with metal gate electrodes.

The toughest nut to crack, experts at the 2005 Symposium on VLSI Technology said, is no longer the high-k gate oxide, but which metal gate electrodes to use—in combination with the hafnium-based high-k oxides—to set and maintain the correct threshold voltages.

And time is running short, making it likely that most companies will not use a high-k solution, at least not in the first go-round of the 45-nm node.

“We’ve got about two weeks to decide on our high-performance process,” said Scott Crowder, director of the 45-nm process development effort at IBM Corp.’s Hopewell Junction, N.Y., center. High-k remains an option, he said, but a solution needs to come soon.

Mark Bohr, director of processor architecture and integration at Intel Corp.’s Hillsboro, Ore., laboratory, said Intel’s microprocessor design teams by this point in the two-year logic technology cycle

would have expected to receive transistor information and layout design rules for the 45-nm node.

“We are really being pressed by the clock,” he said.

If Intel is to continue its normal two-year cycle between nodes, Bohr said, it must make decisions soon about the gate stack, particularly whether to use a high-k oxide with metal gates. And that involves a related choice: whether to use different deposited metals at the N- and PMOS transistors or to rely on a fully silicided (FUSI) process that replaces the polysilicon electrode with nickel or another silicideable metal that can be doped and tuned for the right work functions.

Intel still hasn’t developed a complete high-k oxide, metal gate solution for the 45-nm node, Bohr said, though it is “narrowing down its options.”

Intel has taken multigate devices off the 45-nm table, Bohr said. Two years ago, multigate transistors were seen as an alternative for improving drive current, in case a high-k solution was not ready for 45 nm. Among

the multigate challenges, he said, is controlling the width of the narrow fin.

While it would be possible to continue to use the conventional nitrided gate oxide with a polysilicon gate electrode for the 45-nm node, Bohr said, “in my view, we can do better than that.”

That makes it imperative to find a good

metal for the gate electrode. “We are still interested in FUSI,” Bohr said, partly because that method has shown less process complexity than depositing two different metals at the gate electrode. “It is hard to get the exact work function we need with FUSI, but it is not impossible.”

Frustration on metal progress

Technology managers here said they are encouraged by the progress shown with the hafnium-based oxides, in terms of reliability, leakage mobility, and electrical oxide thickness. What is lacking is the ability to fix and maintain the V_t , which depends on getting the right metal electrode to set the work function as near to the edge of the bandgap as possible.

At the VLSI Technology symposium, several technology managers agreed that the Kyoto meeting demonstrated little progress in the search for a metal gate. Sufi Zafar, an advanced gate dielectrics researcher at IBM’s Thomas J. Watson Research Center in Yorktown Heights, N.Y., said her industry “thus far cannot find the right metals. All of these companies are doing [wafer] splits for four years now, all over the world, and yet we still only have midgap metals. We need to come up with methods to get there faster.”

Zafar has proposed that companies adopt research methods—based on theories developed in the 1960s but stumbled upon only recently—that would provide understandable data to the gate oxide/metal gate research community. “We have to get the industry to focus on what the prob-

CONTINUED ON PAGE 10



IBM's Fried: HOT's a contender for 45 nm.

Sony, Toshiba tip DRAM prototype

By Yoshiko Hara

Sony Corp. and Toshiba Corp. have jointly developed an embedded-DRAM cell measuring 0.069 square micron in 45-nanometer CMOS technology. The companies presented their on-chip memory for high-performance system-on-chip devices at the 2005 VLSI Symposia here last week.

Sony and Toshiba are now in the third phase of collaboration, having jointly developed 90-nm and 65-nm process technologies. They have

been collaborating on 45-nm process technology since February 2004.

When the embedded-DRAM scales down, the capacitance of the deep-trench capacitor decreases. To compensate for that decrease, the R&D team introduced a bottle-etching process combined with a structure, dubbed a Locos collar, that enables the trench to form in a bottle-like shape. The trench, therefore, is wide but has a narrow mouth. This shape increases the surface area of the deep trench, resulting in larger capacitance.

In addition to the trench’s bottle-like shape, the companies used a high-k-node dielectric material (Al_2O_3) in place of conventional nitride-oxide insulation.

The DRAM prototype’s data retention characteristics—the key index of DRAM performance—are almost at the same level as that of 65-nm embedded DRAM, the team said.

To improve performance and establish full compatibility with the logic process, a hybrid shallow-trench-isolation structure and a new strap structure have also been introduced to the embedded DRAM.

In a functional test of a 256-kbit embedded-DRAM macro, a yield rate of 61 percent was obtained, the team reported.

The companies have spent a total of about 20 billion yen (\$183.4 million) to develop the process. About 150 engineers from both companies plan to gather at Toshiba’s R&D center and Oita fab in March 2007 to establish the key technologies for the 45-nm generation.

Key technology of 45-nm embedded DRAM cell

	65 nm	45 nm
Cell size	0.11 μm^2	0.069 μm^2
Capacitor insulation	Thinner NO_2	High-k (Al_2O_3)
Process for deep trench	TEOS collar	LOCOS collar, bottle etching
STI structure	HDP	Hybrid (SOD+HDP)
Strap	BS	USBS
Additional process after forming deep trench	Silicide block	None

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News

45-nm decisions

FROM PAGE 8

lems are, which are fixed charges in the oxide and setting the work function with the metal gate. Right now, the numbers [from different companies] are all over the map; it's all very process-dependent."

Jorge Kittl, a Texas Instruments Inc. gate oxide researcher assigned to the Interuniversity Microelectronics Center consortium in Leuven, Belgium, presented results from an IMEC study of FUSI metal gates that he said showed "good progress, though we haven't seen any breakthroughs. Interest is high from the companies needing a low-power solution, but for the high-performance applications we still need to get the threshold voltages lower, to get a little more swing on both the NMOS and PMOS."

Byoung Hun Lee, an IBM assignee to International Sematech who manages the advanced gate stack program, said he believes that "by the end of this year we can deliver a high-k/metal gate solution to our Sematech member companies. There is a fair chance that we can deliver it in time for companies to use high-k at the 45-nm node by 2007."

Lee added that Sematech has "identified, but has not disclosed," a good candidate metal for the PMOS gate electrode.

The search for the appropriate metal for the NMOS metal gate, "is a little more difficult," he said. While many companies favor a FUSI approach, Lee thinks FUSI is "not manufacturing-friendly."

"As dual-metal-gate deposition gets more and more difficult, then FUSI looks more promising," said Hans Stork, chief technology officer at Texas Instruments. "We haven't made a firm decision, but FUSI is a reasonable candidate."

TI's road map calls for SiGe-induced strained silicon to be introduced for the high-performance 65-nm process, accomplished by depositing silicon germanium at the source and drain of the PMOS and adding a nitride capping layer at the NMOS, much as Intel does. For the 45-nm node, a metal gate could be used in combination with a conventional plasma-nitrided oxide, thus reducing polysilicon depletion and boosting performance. Then, at 32 nm, a high-k oxide could be combined with the metal gate electrode.

TI's goal of changing one material per node is aimed at reducing risk, Stork said.

Ming-Ren Lin, director of the technology research group at Advanced Micro Devices Inc. (Sunnyvale, Calif.), said a FUSI metal gate would remove 4 to 5 angstroms of electrical oxide thickness,

compared with a polysilicon gate on top of a nitrided oxide. "Nobody has claimed victory on a complete high-k and metal gate solution. That would be way too aggressive [for the 45-nm node]."

"There still is work to be done on integrating high-k with the metal gates," said Luc Van den hove, vice president of silicon

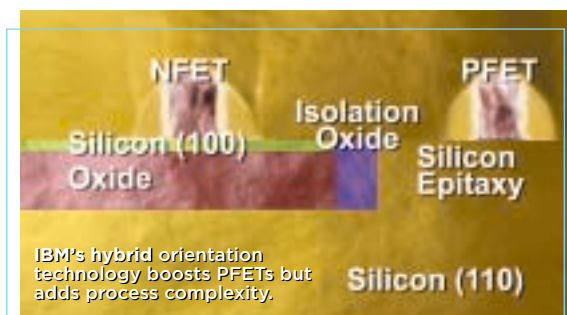
silicon in the PFET regions, with 100-oriented silicon for the NFET.

Is the extra process complexity worth the roughly 14 percent ring oscillator performance gain?

Meikei Ieong, a senior manager of exploratory device research at IBM, said selective epitaxial growth of 110 silicon at the PFET regions may sound difficult. But he argued that the additional complexity compares in difficulty to the added process steps needed to achieve strained silicon: either selective deposition of silicon germanium in the source and drain (the form that Intel introduced at the 90-nm node), or the dual-stress liner approach to strained silicon taken by IBM and AMD.

David Fried, the IBM logic device design manager who presented HOT to the symposium here, said that "HOT is definitely a challenging technology, particularly the selective silicon epitaxy in the PFET areas. For the designers, it means different circuits, because one transistor is in bulk and one is in SOI. But it provides a 30 percent improvement in the PFET on-current, which is huge."

Will IBM bring HOT in at the 45-nm node? Fried said HOT is being evaluated "as a serious contender. It is very product-sensitive. All the materials are conventional, so it's just a materials integration challenge."



process and device technology at IMEC. "People can always make optimistic statements, but in reality this industry is quite conservative and will avoid new approaches for as long as possible."

HOT debate on orientation

With performance at a premium at Big Blue, IBM has developed one process module ahead of the rest of the industry: a hybrid orientation technology, or HOT, that provides a major boost for PFET performance. HOT combines 110-oriented

Intel details all-CMOS WLAN transceiver SIP

Intel Corp. has used 90-nm CMOS technology as the basis for wireless LAN transceiver silicon intellectual property (SIP) that can support both 2.45- and 5-GHz operation.

The SIP, with on-board power amplifiers, low-noise amplifiers and 1.4-V operation, marks another step in Intel's plan to enable anywhere/anytime connectivity, as the company develops the RF capability to achieve that goal. The company described its work last week at the VLSI Symposia in Kyoto, Japan.

"Intel is known for its research and is known for its microprocessors, but the fact that two out of the five papers are from Intel shows how far we've come," said Krishnamurthy Soumyanath, senior principal engineer and director of the Communications Circuits Lab of Intel's Corporate Technology Group (Hillsboro, Ore.). The company presented its paper in session 19 on WLAN RF ICs (www.vlsisymposium.org/circuits/technical.html). Its second paper described a highly linear filter and VGA chain with novel dc-offset and correction in a 90-nm digital CMOS process. Other papers in the session came from

Matsushita, NEC, the University of Tokyo and the Hong Kong University of Science and Technology.

Intel has long advocated using CMOS for RF to deliver multimode radios in a laptop or handset, with the ultimate goal being a form of cognitive radio with a reusable baseband. But, said Soumyanath, while lower-power operation is essential, "it's very hard to do analog circuits at low voltage." Low power must also be combined with lower cost and wider analog bandwidths of up to 100 MHz, he added.

90-nm process tapped

To meet those goals, researchers relied on Intel's 90-nm process and made advances in SIP integration using microstrips, 5-GHz power amp (PA) integration, frequency planning to minimize noise from the PA, short transistor stacks on the PA for low-voltage operation and I/Q mismatch calibration techniques to simplify and speed the production cycle.

While Soumyanath could not comment on product plans, he said that one likely option was to integrate the package with a digital baseband for a fully integrated solution. —Patrick Mannion

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Chip makers' offshore fabs rev to fill consumer orders

As global demand heats up, some see inventories fading, memory shortages looming

By George Leopold and Mark LaPedus
Anaheim, Calif. — A flurry of recent reports indicates that U.S. chip makers are expanding their offshore manufacturing operations to prepare for growing demand.

Intel Corp. is reportedly considering increasing its assembly operations in Asia by adding new sites in India and Vietnam, while chief processor rival Advanced Micro Devices Inc. is considering constructing a third wafer fabrication facility in Dresden, Germany.

The reports come as some chip industry executives are warning of future shortages of memory chips as consumer-driven demand heats up, and as the excessive inventories that slowed the chip market for the past year have been reduced. In addition, a growing number of research houses have raised their IC forecasts for 2005. Citing stronger than expected chip sales, for example, the Semiconductor Industry Association recently revised its annual forecast for global IC sales to a record \$226 billion in 2005.

Meanwhile, still unclear is whether Intel's plans for India involve more than just back-end assembly facilities. The company was reported by *The Wall Street Journal* and others last week to be considering an investment totaling about \$400 million. Intel already has test and assembly facilities in China, and some suggest its India plans could be more ambitious than a test and assembly operation.

Intel is also among the companies considering a move into Vietnam. Asian industry observers point to that country as the next big target for chip industry investment.

A spokesman for Intel declined to comment on reports about the company's plans in India and Vietnam. "I know we've looked at India, but we haven't made a decision," the Intel spokesman said. "It's the same in Vietnam. We look at expanding our plants all the time."

Still, Intel is spreading its wings outside the United States, especially in Asia. Some 75 percent of Intel's business is already generated outside of the United States. "Intel is putting its emphasis on emerging markets," according to a spokesman for the company, referring to Asia, Latin America and Russia.

China's capital

For example, expanding its efforts in China, the company announced last Monday that it will establish a \$200 million venture capital fund in that nation. The Intel

Capital China Technology Fund will be used to invest in companies that complement Intel's technology initiatives in China. "We will invest in Chinese companies to accelerate technology adoption locally and to foster development of innovative technologies with potential for global distribution," said Intel president and chief executive officer Paul Otellini in a statement. Cellular communications, broadband and semiconductor design were cited as areas of initial focus.

Last year, Intel and a Chinese start-up struck a deal on the transfer of manufacturing technology and equipment, believed to be the first such deal that the CPU giant has made in China. The company licensed 0.35- and 0.25-micron CMOS process technology to Nanotech Corp., a semiconductor foundry based outside of Shanghai in Changzhou, Jiangsu Province.

Intel already operates three assembly and testing factories at a site in the Shanghai Pudong New Area in eastern China. In March, the company announced plans to construct a second assembly and testing factory in the municipality of Chengdu in China's Sichuan Province.

Offshore blitz

Meanwhile, Germany's *Frankfurter Zeitung* quoted Hector Ruiz, chief executive officer of AMD, as saying that the chip maker needs to expand its fab operations to meet growing demand and that its Dresden operation is the leading candidate. A decision on AMD's plans is expected by mid-2006, *Frankfurter Zeitung* reported.

The flurry of fab expansion reports comes as chip makers brace for growing global demand, which is expected to be fueled by such consumer applications as multimedia third-generation phones and other mobile applications.

The flash memory business is one industry sector girding for exploding demand as more features are added to mobile phones. An executive from Samsung, a leading memory supplier, warned last week of future memory shortages if vendors stumble in their efforts to shift between NAND and NOR flash memory technologies.

"We're moving from the mobile decade to the mobile consumer decade," Jon Kang, senior vice president of technology marketing for Samsung Semiconductor, told the Design Automation Conference here last week. Kang said the proliferation of mobile devices coupled with the emergence of gadget-filled 3G phones will sharply increase demand for memory.

As a result, memory makers are also looking to expand their operations while scaling down their memory technologies for emerging consumer applications.

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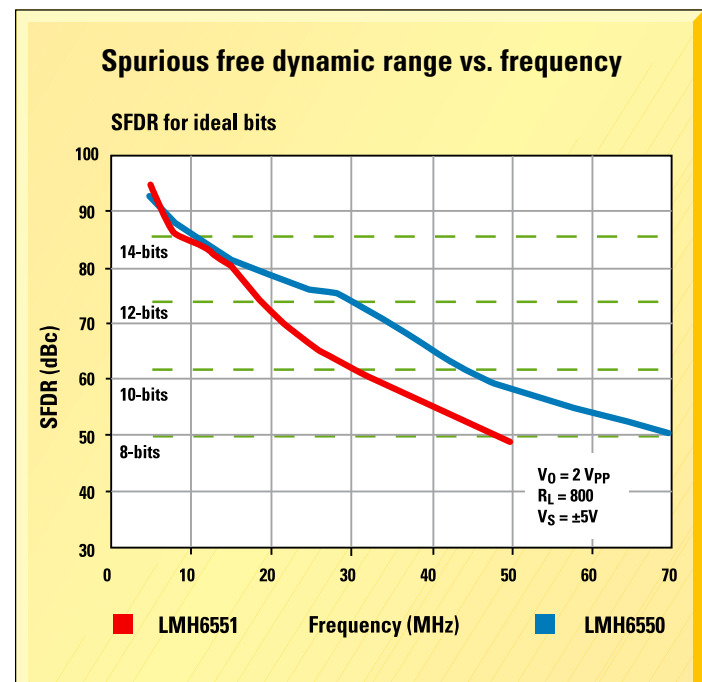
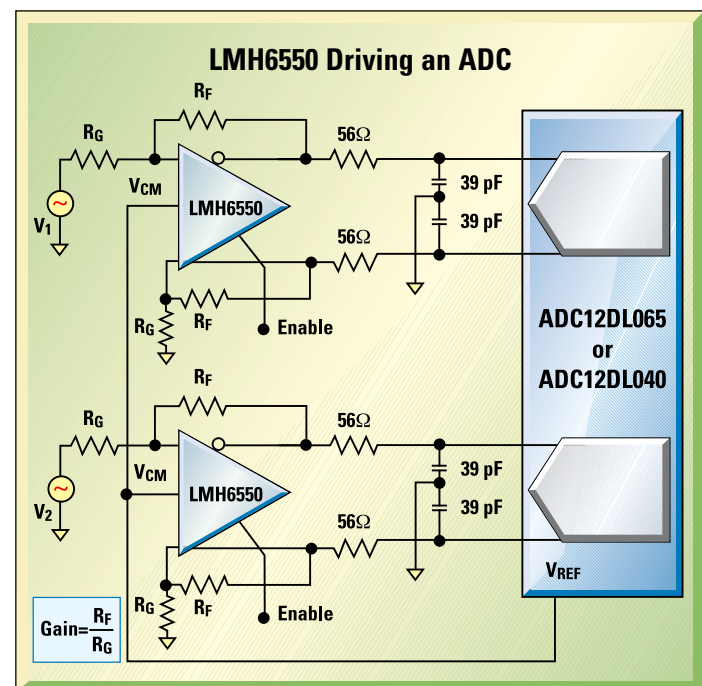
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ESL mainstreams

FROM PAGE 1

chief analyst Gary Smith noted that 27 percent of chip designers are now using internal tools, up from 20 percent in 2001. And the *EE Times*/Deutsche Bank 2005 EDA survey found that system-level design is a key area for internal tool development (see June 13, page 24). **S**

ESL's challenges start with "defining what it is," said Emil Girczyc, CEO of Summit Design Inc., at a DAC panel session. Historically viewed as anything above RTL, what ESL really involves is highly application-dependent, he said.

“The ESL goal is concurrent hardware/software design from a single high-level model,” said Dataquest’s Nadamuni. Dataquest has identified three ESL methodologies: one for processors and memories, one for control logic and one for algorithms, each involving its own behavioral- and architectural-level tools and techniques.

The SystemC factor

ESL techniques such as C-language modeling, transaction-level modeling and algorithm development using Matlab have been around for years. What's different now is that SystemC is bringing high-level

el design techniques to designers who are stepping above RTL for the first time.

One of those is Tom Paulson, principal engineer at QLogic Corp., a developer of Fibre Channel switch ASICs. Just a year ago, Paulson wasn't even sure what ESL was. Since then his company has adopt-

Samsung's ESL challenges

- Lack of measurable performance index to justify the investment
- Too much modeling effort at transaction level
- Embedded software design at transaction level too slow to be behavioral and less accurate than RTL
- Lack of vertical/horizontal interoperability and point tools
- Lack of equivalence checker and TLM coding rule checker
- Too difficult to insert/extract nonfunctional parameters
- Manual function decomposition for hardware/software partitioning
- Lack of common verification suite in different levels of abstraction
- Too many input constraints for behavioral synthesis

Seagor, Seagor Electronics Co., Ltd.

ed SystemC modeling, along with analysis and graphical entry tools from Summit.

“Our RTL design flow is working very well,” Paulson said. “But our algorithms are becoming more complex, and we wanted to look into architectural modeling.”

After a successful evaluation that involved creating a SystemC model of an

existing ASIC, QLogic brought SystemC modeling into its production design flow, where it's used to evaluate such features as buffer size, steering algorithms, transmit algorithms and service delivery.

The result is better design quality, Paulson said, but QLogic is taking it slow.

“We’re using the SystemC model to evaluate architectural features, but we’re not looking at this point to move it to RTL.”

Samsung has been at it a little longer and is getting closer to the Dataquest vision of concurrent hardware/software design. Samsung has been using SystemC transaction-level modeling since 2003.

Last year, Eo said, the company set up a “virtual platform design methodology,” with presilicon software development and verification, architectural exploration and performance analysis, and hardware/software co-verification.

Samsung is developing tools for embedded software optimization, low-power optimization and hardware/software co-design, and it is building links to external tools.

But Eo's list of ESL problem areas is long. It includes a lack of a measurable performance index to justify tool investments and the lack of equivalence checking. And "it takes so much effort to create the models that all the advantages ESL has could be wiped out by the modeling effort," he said.

Other designers are developing their own ESL strategies. Sriram Sundararajan, senior staff member at Texas Instruments Inc., called SystemC transaction-level models useful for architectural definition and validation, but he added that “tools are lacking in this area, which is the most important part of system design.”

Using an internal approach along with open-source tools from OSCI, Sundararajan said, TI has developed high-level SystemC models that transfer tokens rather

CONTINUED ON PAGE 17

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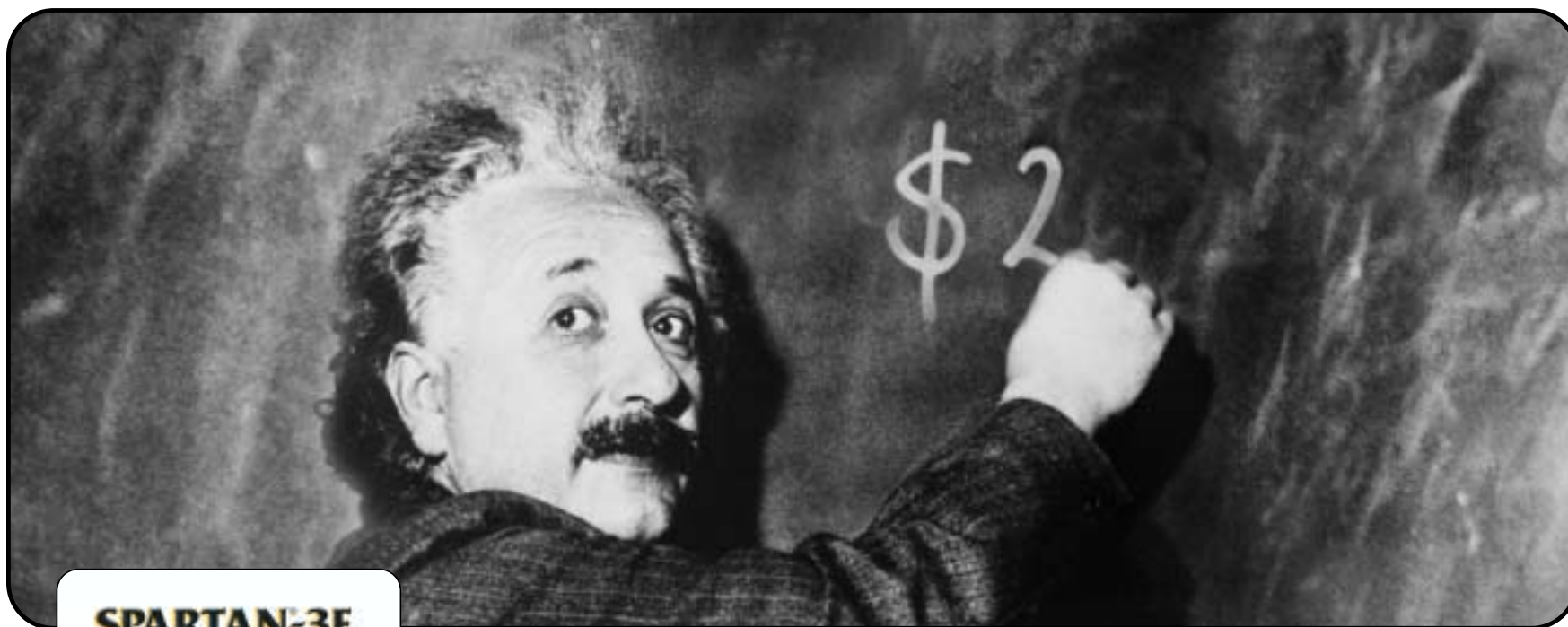
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News

EDA comes to DFM table

But vendors, EEs differ over design for manufacturing

By Ron Wilson

Anaheim, Calif. — In a rare display of comity, EDA vendors and process engineering experts sat together on a panel at last week's Design Automation Conference here, but unfortunately talked past each other on the subject of design for manufacturing.

Panel chairman Naveed Sherwani, president and CEO of Open-Silicon Inc., opened the discussion with the observation that, with the possible exception of ESL (electronic system-level design), no acronym was being used as frequently—and as frequently in vain—as DFM. Arguing that the term had already drifted from any technically useful meaning, Sherwani quoted industry commentator John Cooley as saying that DFM had come to stand for “dollars for marketing.”

The responses of the panel members to Sherwani's statement demonstrated that even among vendors who take the term seriously, there are major disagreements about just what design for manufacturing should entail. And there is a yawning gap between what EDA vendors mean by DFM and what process engineers warn they should mean.

For example, while one vendor representative spoke of correcting problems with mask features, another focused on the improvement of yield models. Still another argued for rule-based, rather than model-based, DFM. And the lone equipment representative on the panel countered that such improvements, while needed, would not be sufficient if the industry didn't provide calibrated process models.

Atul Sharan, president and CEO of Clear

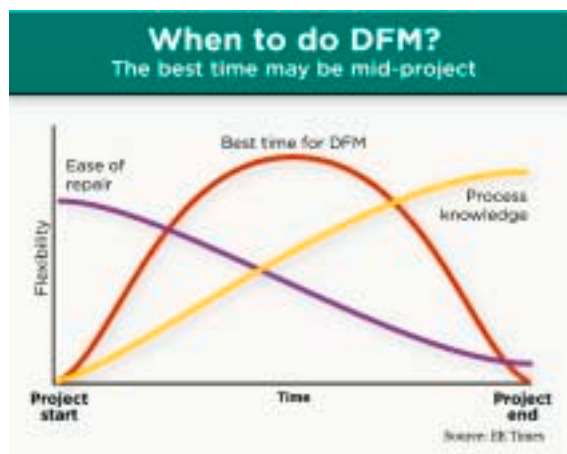
Shape Technologies Inc., for instance, briefly discussed the problems that deep-subwavelength lithography is imposing on the design of critical layers. It's commonly understood that we have to heavily modify the features on masks to produce the features described in the design data, Sharan said. But what's less understood is that this reticle enhancement technology (RET) doesn't necessarily produce what we had in mind even then. “With RET we can only do what is possible—what we can compute and fit within the allowable space,” Sharan warned. “We can't always do what is necessary to produce the features we wanted, especially over the range of focus variations in a real fab environment.”

Sharan suggested that the only safe solution was to develop a tool that could predict the actual features on the die, taking into account process variations, and then extract electrical data from them.

Ponté Solutions Inc. president and CEO Alex Alexanian suggested a step further over the precipice. Dismissing out of hand the possibility of producing first-time-yielding designs from a 1,000-page design rule book with mutually contradictory and hopelessly restrictive rules, Alexanian called for not just feature simulation but also a statistical metric that would encompass both random and systematic failure models, and could be integrated directly into the design methodology. Designers must be given information about what their yields will be on a feature, he argued, not simply advised not to use it.

The distinction between random, defect-driven and systematic, feature-driven yield issues was emphasized by PDF Solutions Inc. senior director for

DFM solutions Carlo Guardiani. “Defect-induced yield has been essentially flat at around 90 percent for several generations,” Guardiani observed. “But feature yield has been dropping continuously.” Guardiani showed a foil estimating no more than 60 percent feature yield at 90 nanometers. “But most so-called DFM tools today address defect-caused problems with techniques such as line spreading or via doubling. These techniques, if



not done with sensitivity to the issues that cause features to form improperly, can actually increase overall failures by causing features not to form.”

Guardiani called for a two-pronged effort that would strive to identify yield-sensitive features from the design database; identify pattern sensitivities in the fab process; then compare the two. Only by calibrating yield models based on actual process data and then applying the models to critical patterns in the design would it be possible to identify, prioritize and selectively correct the potential problems before tapeout, he argued.

A sharply different view was voiced by Xilinx's Peter Rabkin, who advocated rule-based, rather than model-based, DFM. “This has to be an iterative process within the design,” Rabkin said. “There is a basic problem that the opportunity to identify rule violations and repair them is clearest early in the design. But this is the time when the process is the least mature and you know least what the rules will be. So the most effective time for applying DFM rules is in the middle of the design, when fixes can be proposed and prioritized without disrupting the layout hierarchy, and when the process has matured enough for the rule set to be reasonably complete.”

While attention among the EDA vendors focused on statistical models that attempted to predict yield, a chill breath of reality was offered by the one representative from the equipment industry on the panel, KLA-Tencor Corp. program manager Harold Lehon.

Lehon agreed with Sharan and Guardiani that routines would have to be integrated into existing flows that would open up space for aggressive RET features in critical nets, and that electrical parameters would have to be extracted from real, process-perturbed shapes based on process models rather than from simple lithography simulations. But he warned that this would not be enough.

Eventually, Lehon said, calibrated process models would be necessary to estimate the result of design features accurately and feed that data back into the design flow. Such models would make possible layout tools aware of the impact they were having on the lithography process, and RET tools aware of the design intent.

But these models will not be simple or fast. “Hardware acceleration will be required to accomplish this,” Lehon said.

ESL mainstreams

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than data. “These models come up quickly, and even without RTL, we can get a lot of insights into the architecture,” he said.

Qualcomm Inc. uses SystemC for architectural characterization, said principal engineer Suhas Pai. It also uses a “virtual platform” for IP modeling, a system-on-chip testbench for simulation and a transaction-level co-emulation approach.

SystemC modeling helps design become a more “concurrent” process and allows early architectural exploration, Pai said, but Qualcomm designers “really could have used training on how to use the language features for more efficient modeling, because the language is so rich.”

Terry Doherty, principal engineer at Emulex Corp., has been doing system-level modeling for about three years. He uses SystemC transaction-level models for architectural analysis and exploration for

the company's storage-networking chips.

With SystemC, Doherty can optimize buffer sizes, implement new protocols, make hardware/software trade-offs and ensure that FIFOs won't overflow. He uses commercial tools for analysis and debug but proprietary tools for analyzing protocols. His wish list includes tools to prove RTL code meets system requirements, along with better data management.

STMicroelectronics described a home-grown Matlab-to-RTL flow that was used to design a 135-Mbit/second, DVB-S2 complaint codec. The flow uses formal methods to verify the RTL against the high-level description. ST is also developing an automated synthesis flow, said Pascal Urard, signal processing senior expert.

There are gaps in these flows, Urard noted, including synthesizable code generation from Matlab to SystemC, formal proof for the generated C and RTL code, and code checkers at many levels. The learning curve can be steep, he noted.

As for SystemC itself, Charles Pilkington,

senior staff R&D engineer for SoC platform automation/central R&D at STMicroelectronics, would like enhanced simulation and debugging definitions.

“System C is good but not perfect,” said Reinaldo Bergamaschi, research staff member for the System-Level Design Group at IBM's Thomas J. Watson Research Center. He called for more involvement of the “open development” community and for better links between SystemC methodologies and RTL flows.

EDA vendors respond

Earlier this month, the EDA vendor community rallied behind the SystemC transaction-level modeling (TLM) standard 1.0, which defines application programming interfaces and a library that implements a foundation layer on which interoperable transaction-level models can be built (see June 6, page 18).

One DAC forum involved ESL providers Summit, ChipVision Design Systems AG, Calypto Design Systems Inc.,

Critical Blue and Forte Design Systems Inc. Summit's Girczyc outlined an approach to ESL that is driven by application software rather than hardware.

Stan Krolkoski, CEO of ChipVision, presented his company's work with ESL power estimation. He said one customer had attained a 70 percent power savings.

Mike Meredith, vice president of technical marketing at Forte, claimed that six of the top 12 chip vendors use Forte's Synthesizer SystemC tool and that 20 designs are in production with it.

Forte also took part in a novel benchmark at DAC. John Cooley, moderator of the E-Mail Synopsys Users Group, bet Forte VP Brett Cline that fewer than half of the respondents to Cooley's Design and Verification survey would say they planned to use SystemC in six months. The loser would have to don a chicken suit.

Cooley and Cline walked into a demo suite to review the survey results. Cline walked out wearing the feathers.

— Contributions by Nicolas Mokhoff



News

Beyond the Horizon

U.S. broadband

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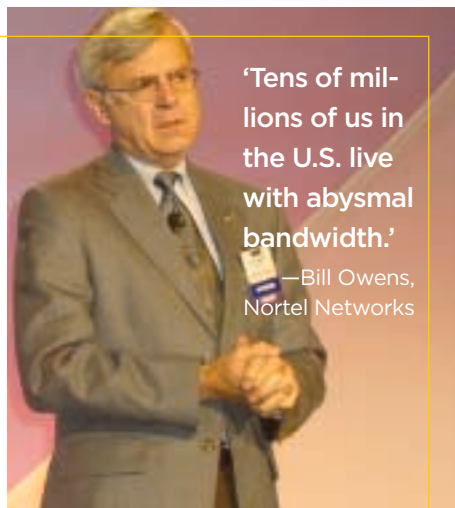
won't make it to Black Forest anytime soon.

"At least Adelphia came out and said they wouldn't be building out for years," Ryd said, "but Qwest kept giving me different stories" about when its DSL access multiplexers would be in place. "It seems the sales folks never really talked to those making the provisioning decisions, so no one would give a solid 'No.'"

He and Doyle are desperate. They've resorted to signing up for 802.11 Wi-Fi service at a local coffee shop, Ryd said, because they "just can't tolerate 56k any longer."

So where is the broadband Valhalla we were promised in 1996?

The mild upturn in carrier fortunes at the recent Supercomm show in Chicago could not disguise industry leaders' concern over U.S. residential broadband penetration trends. In a keynote speech, Tellabs Inc. chief executive officer Krish Prabhu cited International Telecommunications Union (ITU) statistics showing



'Tens of millions of us in the U.S. live with abysmal bandwidth.'

—Bill Owens, Nortel Networks

that "we are now in 16th place [in broadband penetration] worldwide, and the numbers are still trending down."

"There are tens of millions of us in the

Service tiers and pricing worldwide

Entry-level broadband		• ADSL, DOCSIS modems 512-kbit/s to 10-Mbit/s downstream, 2.5-Mbit/s upstream
Japan		• Ubiquitous but obsolete, sub-\$20 a month if available
Korea		• 12 million lines, \$25/month
United States		• 62 million subs, more than 100 million residences passed, \$30 to \$50/month
Second-generation broadband		• ADSL2, ADSL2+, VDSL, 2G DOCSIS, GPON, EPON; 10-Mbit/s to 52-Mbit/s downstream, 10-Mbit/s up
Japan		• 15.3 million subs, 30 million residences passed, \$22/month fees
United States		• Early stages, under 1 million subs, average \$50/month
Ultra-broadband		• Active optical fiber to the home 100-Mbit/s and greater downstream, 50-Mbit/s and greater upstream
Japan		• 2 million subs, 38 million residences passed, \$30 to \$45/month
United States		• Virtually nonexistent

Source: EETimes

U.S. who live with abysmal bandwidth," Nortel Networks chief executive officer Bill Owens said during a Supercomm presentation. "Our vision of regulatory policy is virtually nonexistent."

In his article "Down to the Wire" in the May/June issue of *Foreign Affairs*, Thomas Bleha, a former foreign-service officer in Japan, said that no U.S. carrier has revealed plans that can match Japan's nearly universal availability of 20-Mbit/second broadband for \$22 a month or that country's plans for 100-Mbit/s fiber-to-the-premises that will provide 30 percent of its citizens with active-fiber connections for between \$30 and \$40 per month by 2006.

If the President's Information Technology Advisory Committee worked with carriers to develop usage plans for existing dark fiber, Bleha asserts, basic broadband access could become universal in the States, for a subscription fee of \$20 a month, by 2010. By that same year, he says, two-thirds of all U.S. households could have the option to switch to 100-Mbit/s fiber services for \$30 to \$35 a month.

Failure to drive this goal as national policy could make U.S. companies fundamentally uncompetitive with most Asian and European nations within a decade, Bleha warns.

Verizon Communications Inc., SBC

Communications Inc. and BellSouth Corp. are not waiting for a sign from the White House; each is rolling out passive optical network (PON) installations to enable multimegabit customer access speeds at minimal cost to the carrier. Strategies range from all-PON fiber-to-the-home, used in Verizon's FiOS, to fiber-to-the-node architectures that employ twisted-pair copper in short VDSL loops.

Still, critics compare the PON efforts unfavorably with the efforts to provide 100 Mbits/s to all citizens in Japan and South Korea via active fiber.

"We definitely see more interest in Asia for the newest upgrades for our broadband routers," acknowledged David Boland, senior manager for access routers at Juniper Networks Inc. But don't count out the States, Boland said. "Have Japan and Korea and other countries gained momentum by having a policy to bring fiber to every user? Of course. But you can't assume as a result that the U.S. has become a broadband no-show."

Telecom equipment OEMs and semiconductor suppliers agree that the incumbent local-exchange carriers and cable multisystem operators have become stalled at current generations of asymmetric digital subscriber line (ADSL) for twisted-pair access and at Docsis cable modems for hybrid fiber-coax systems.

Lothar Pauly, chief executive of Sie-

mens AG, said that carriers are being too conservative when they talk about "triple play" services' uniting voice, data, and video. "Triple play is a great defensive play, but a grand slam is what puts points on the board," Pauly quipped.

An all-encompassing vision must consider local- and wide-area wireless services as part of an integrated whole with other broadband consumer offerings, Pauly said. Phone, cable and utility companies, he said, are not thinking long term when they develop services as defensive measures.

Every carrier today has a different view on how broadcast and streaming Internet Protocol TV channels will be carried, and each approach has direct implications for the bandwidth that must be delivered to the user.

PON: No paradise, no panacea

With region-wide programs like Verizon's FiOS and SBC's Lightspeed, PONs are being adopted with fervor by carriers looking for a low-cost way to drive fiber speeds closer to the customer. By limiting active-fiber switching to a neighborhood node and using passive fiber components in the last mile, PON promises to give carriers a faster path to profitability than traditional FTTH programs. PON also can be used in conjunction with twisted-pair

CONTINUED ON PAGE 20

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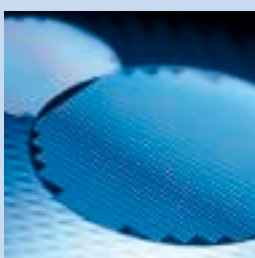
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Never stop thinking.



News

Beyond the Horizon

U.S. broadband

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schemes that use copper wire from the home to the optical line termination device, and the faster speed of the backbone allows use of faster DSL alternatives, such as VDSL and VDSL2, to accelerate customer download speeds to 25 or 50 Mbits/s.

For some business and even residential networks, it might make sense to use active switched fiber from a broadband loop carrier, as Occam Networks Inc. and Telco Systems Inc. have demonstrated. Utility companies have found such networks in "greenfield" residential builds, where they can also use the optical terminal for meter reads.

But PON is hardly a silver bullet.

Double play was an easy step up, even when extended to digital cordless handsets, said Faraj Aalaei, CEO of Centillum Communications Inc., which makes xDSL chips and also has formed an optical-components group to design PON chips. But video support in triple-play requires a new way of thinking about how content is delivered, Aalaei said.

"There are different approaches for

CONTINUED ON PAGE 76

A chronology of broadband milestones

2000-2002	Japan's Information Technology Strategy Council creates conditions for providers to offer universal fiber to the curb; NTT offers active-fiber fiber to the premises in Tokyo and Osaka
2001	WiMax Forum formed, based on IEEE 802.16 work
2002	ATM-over-PON, broadband PON rollouts
2003	Japan shows more interest in Ethernet-based EPON and GEON than in the European-developed APON and BPON
March-May 2004	Teknovus, Passavé offer EPON chip sets
June 2004	Broadlight, Freescale offer BPON chip sets
June 2004	Texas Instruments proposes UniDSL solution for VDSL2 and ADSL2+, but no silicon until mid-2005
Oct. 2004	STMicroelectronics samples ADSL2+ chip
Dec. 2004	Ikanos samples prestandard VDSL2
Jan. 2005	Verizon announces first communities for fiber-to-the-premises project called FiOS; SBC and Microsoft announce Project Lightspeed as vehicle to test Microsoft TV for IPTV delivery
March 2005	Infineon samples ADSL2+ chip
April 2005	Analog Devices demonstrates ADSL2+ bonding
May 2005	Occam Networks, using Telco Systems switches, proposes active fiber instead of copper from a broadband loop carrier: low-cost active fiber to homes?
May 2005	ITU completes work on VDSL2 standard; Infineon, Conexant announce chip sets
May 2005	Broadlight and Freescale disclose GPON plans; Freescale and Alcatel to share chip-level IP
May 2005	Intel and Alvarion demonstrate working WiMax networks at Interop
June 2005	Broadcom samples combo ADSL2+/VDSL2 device
June 2005	SBC announces delays in Lightspeed rollout

Source: EETimes

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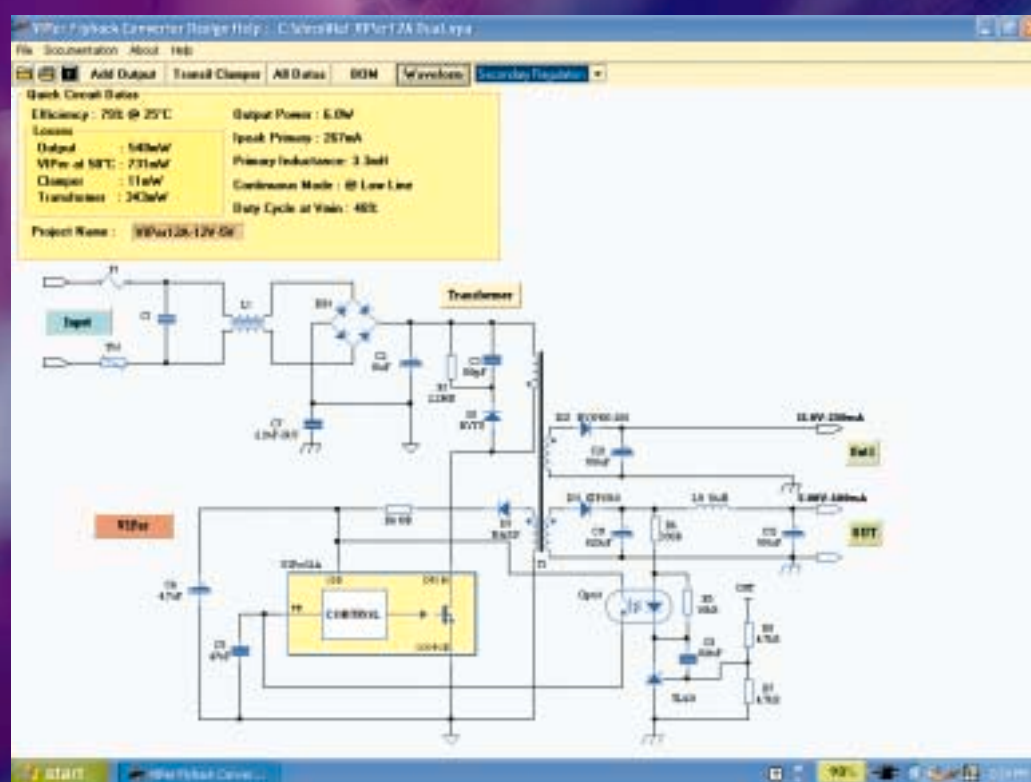
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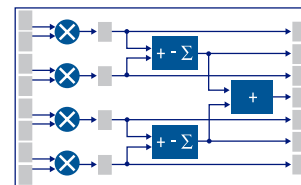
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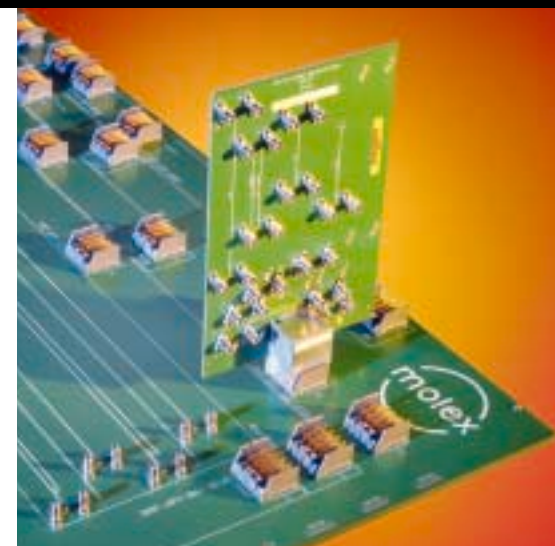
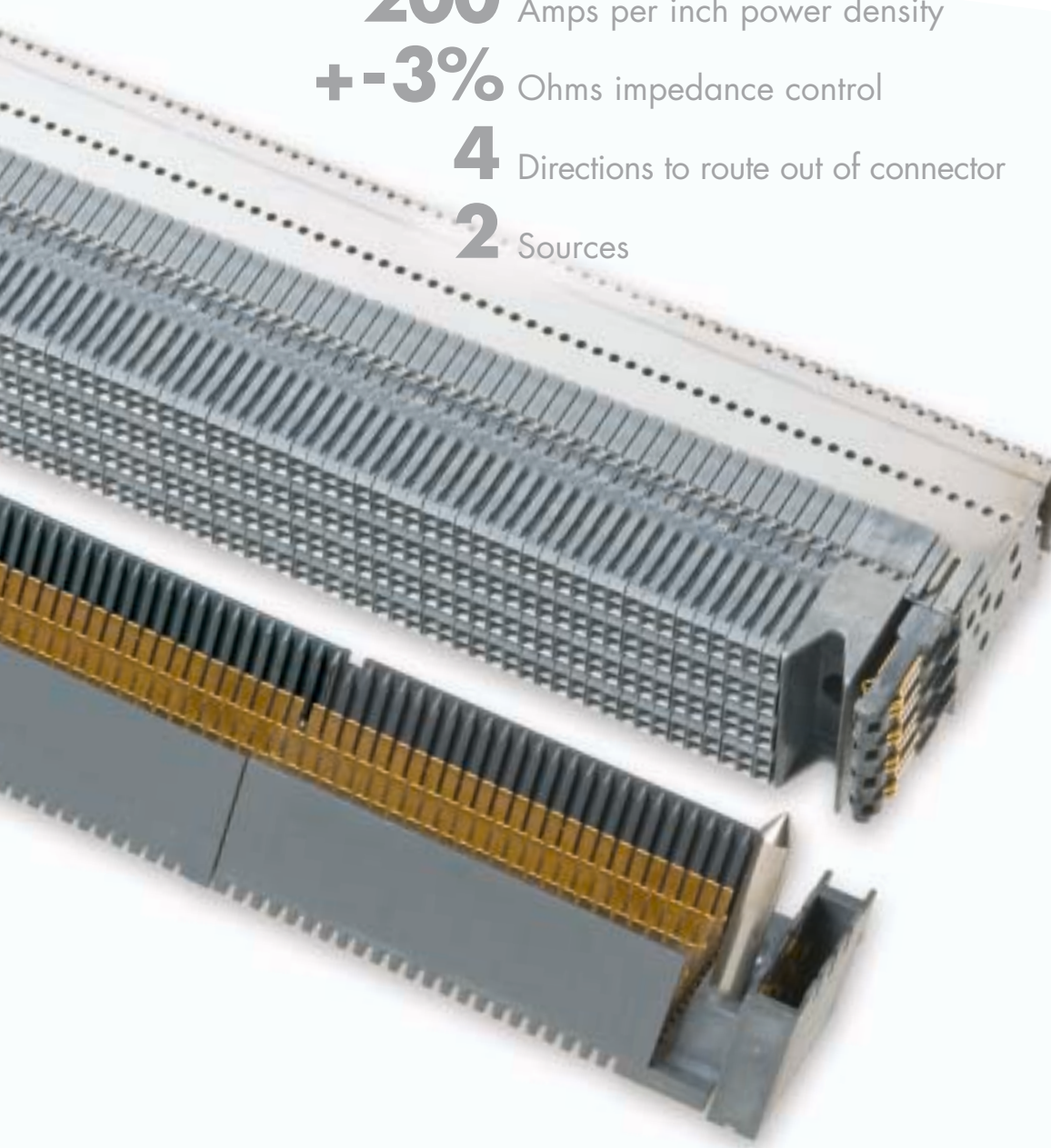


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—□□□□ News □□□□—

The interview

Prof bemoans loss of the long view

By Patrick Mannion

Inspired by Thomas Edison, he built his first radio at the age of 10, fascinated by the fact that he couldn't see the radio waves, yet the information was still there. Now a professor at Virginia Polytechnic Institute, Jeff Reed has authored books on wireless communications, most recently tackling ultrawideband signaling. Here, Reed shares his vision of the future for wireless, as well as his thoughts on the state of U.S. education, U.S. students and the engineering profession in the context of the global economy.

**Jeff Reed****Born**

July 30, 1957, Bakersfield, Calif.

Education

BS, MS, PhD; University of California, Davis, 1979-1987

Experience

- Signal Science Inc., 1980-1986
- Private consultant and part-time faculty member at UC Davis, 1987-1992
- Professor, Virginia Polytechnic Institute's Bradley Department of Electrical and Computer Engineering, 1992-present
- Director, Virginia Tech Mobile and Portable Research Group, June 2000 to June 2002; currently deputy director

Published books

- *Software Radio: A Modern Approach to Radio Design*, 2002
- *An Introduction to Ultra Wideband Communication Systems*, 2005

Awards

- Virginia Tech College of Engineering Award for Excellence in Research, 2001
- SDR Forum Outstanding Industry Contributor Award, 2004
- Named an IEEE fellow this year for his contributions to software radio and communications signal processing and for leadership in engineering education

EETimes: Why did you become an engineer?

Jeff Reed: I just love to make things. I dabbled in chemistry until one of my projects blew up, and then I decided to switch fields. Early in high school I built a little wireless transmitter and tapped my sister's phone. She was in high school at the time and was starting to get interested in boys, so that made it particularly fun.

EET: When did you realize you wanted to be a professor?

Reed: I didn't know I was going to be a professor until I was doing my graduate work. I really enjoyed the teaching and mentoring aspects. My "product" is my students. There are few professors whose research is more important than their students.

EET: Is the quality of students getting better or worse?

Reed: That's a complex question to answer. I find the math skills are not what they should be, but their computer skills are getting better with time. That's been the way for some time. But compared with their international counterparts, their math skills are weaker.

EET: How can they compete globally?

Reed: I think even more than math skills is the attitude of thinking long-term, strategically. This [lack of strategic thinking] has infected not only students but industry and government-based research. They think, "Get the A, get the degree" rather than "What am I learning here?"

EET: What about foreign national students?

Reed: The number of domestic students has declined steadily over the years, if you discount the brief impact of the recession. The ratio of international students continues to increase.

EET: How would you address that?

Reed: It's a cultural thing. It's a culture internationally where education has prestige in itself, whereas in the U.S. we tend to be money-driven when appraising self worth. I'm not sure how we address that. It's a big problem. It's a disadvantage in the global environment, but it's also a disadvantage in the long term.

Right now the job market for students in wireless communications is pretty good, and much of it [for domestic students] is driven by the military buildup. But the economy is coming back, and the commercial companies are getting out there and hiring again.

We're going to see a shortage of engineers—it's right around the corner—and it will have a significant impact on national security. The DOD buildup took place during the worst job market for engineers in over 30 years. But now the market is strengthening, and I'm very concerned about national security and the DOD specifically, but also about [the implications] for the overall economy.

EET: Should the U.S. increase H-1B visas?

Reed: I think that's going to happen, not now but in about two years.

EET: Advice for domestic students?

Reed: They should take courses that will ground

them well in the fundamentals, since they will likely shift jobs many times over the course of their career. Good students really should consider grad school; it pays. Also, having international experience is a big plus. That's the difference between being a successful student now vs. 10 years ago.

EET: And for current working engineers?

Reed: The job market is getting better, and those who keep up their skill levels and are flexible will do much better. For example, software programmers have experienced compression in their job functions. They're doing things that would've been done by graduate students 15 years ago but are now being delegated to undergrads or

non-degreed workers, so in order for them to maintain their relative position within the organization, they need to develop more-sophisticated and broader skill sets.

EET: What projects excite you at Virginia Tech?

Reed: One thing we're doing is creating a software-defined ultrawideband receiver. We're using that to look at ways to do new modulation and MAC [media-access control] design. Of course, our open-source SCA [Software Communications Architecture] has been a big hit for us [[search www.eetimes.com for article ID: 29100148](http://search.eetimes.com/article/ID:29100148)]. Over a dozen companies looked at this for inclusion in their products. We're also looking at low-power software radio design and using SCA for rapid prototyping.

EET: What are the drivers for software-defined radio?

Reed: There are different drivers for the military and commercial markets for SDR. The military is looking for code portability—being able to transfer a waveform so that their systems will be compatible with each other.

But for the commercial markets, the three most important things are cost, cost, cost. What's driving the trend toward SDR here are time-to-market and reduced silicon content for multimode systems. They really don't care about waveform portability: you're not going to run your Ericsson code on a Nokia handset.

EET: Anything in common between the two markets?

J.R.: I think there's some synergism. I think the military will start adapting some commercial principles. Rapid prototyping is very important to them, and I think they'll be more focused on that and less on code portability in the coming years because some technologies such as FPGAs really don't lend themselves to code portability. FPGAs will play an increasing role in radio design, particularly as regards lowering the power consumption. Also, you care less about code portability when you can redo it very quickly. This could be one of the killer apps for SDR—rapid time-to-market with less manpower.

EET: What do you think of ultrawideband?

Reed: UWB is exciting, but I do also have apprehensions about it in terms of power consumption. You need to bring that down to get the full realization of it.

I think UWB may prove useful in ways that people are not yet addressing. Most of the attention has been on the high data rate. Yes, you can get short range and high data rates with UWB—but you also have [IEEE 802.11n] coming down the pipe for that. UWB does give you additional capabilities, such as precise location, and the more bandwidth you have the better you can do locationing, so it does bring to mind impulse systems. So, I think high data rate will be a market in the long term. The lower-data-rate applications—through-wall radio, sensor networks, tag technology and locationing—could happen first.

EET: Will UWB overlap with current technologies?

Reed: You can buy pre-11n equipment now in Circuit City with data rates that you'd have a hard time finding applications for. But low-data-rate, low-power sensors embedded everywhere—those have, in all likelihood, the potential to be revolutionary, at least in the short term. ZigBee and motes [miniature sensor networks], I think, can make a big impact in the future. Also interesting is the work that's being done with pathogen chips.

EET: So, when will we see commercial SDR?

Reed: I believe we'll see technologies come out by the end of this year, though we have it in the basestation, but the full potential of SDR is when both the handset and the basestation are software-defined and flexible.

CONTINUED ON PAGE 26

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News

The interview

Jeff Reed

FROM PAGE 24

EET: SDR in the handset—is that really feasible?**Reed:** Not with current technologies. It's difficult to do and not cost-effective, but we're getting there. [Enabling technologies include] low-power FPGAs, low-power DSPs and programmable ASICs.**EET:** What about the RF front end?**Reed:** That's harder. MEMS [micro-electromechanical systems] have a lot of promise there. You can do smart antennas with MEMS through impedance matching; you can switch in and out RF front ends without incurring substantial losses. You can have flexible and high-performance tuning circuits, with extremely high Qs in the filters. A/D conversion resolution is not set by the signal itself but by the amount of interference in the environment. So, with a higher bandwidth [in an SDR], you need a higher sampling rate—and so you burn even more power.**EET:** Is there a difference between commercial and military RF requirements?**Reed:** Yes, the military guys want to go anywhere in frequency (dc to daylight). Commercial guys have a few select bands that they're restricted to. But 10 years down the road, those restrictions will be less; the FCC is going to be much more flexible in the ways that they use the spectrum. So the power issues will become worse for them, as they'll need even more flexibility.**EET:** What do you think of cognitive radio?**Reed:** It's quite interesting and is one of the big emerging research issues: It's tomorrow's MIMO [multiple input, multiple output]. MIMO is still a big research issue, but frankly I think it's overinvestigated at this point.

While you can argue that cognition has been with us for some time—i.e., sensing interference and moving off-channel—I think it'll become much more sophisticated and more methodical in the approach,

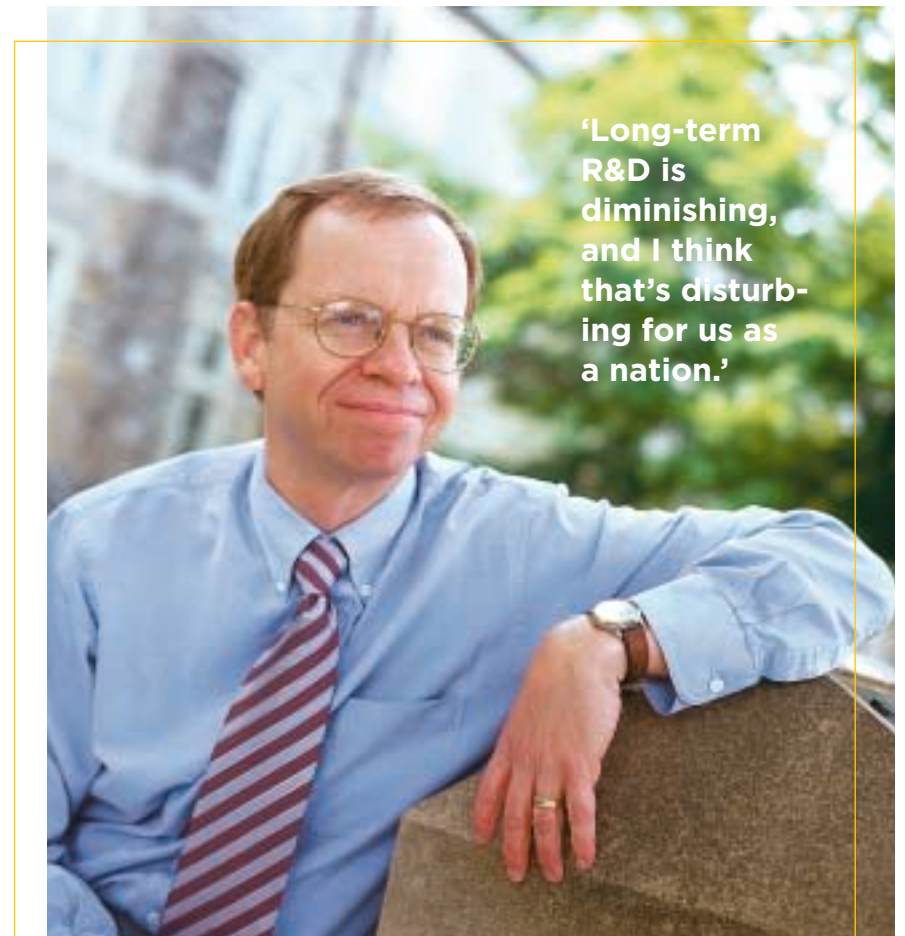
as well as with respect to the system implications of adaptive systems that run from across the wires.

It's a very complex problem. We need to look at interference temperature sensing as well as managing the spectrum—being able to determine the existence of other signals in the spectrum, giving priority to certain signals and sharing that knowledge around the network, and being mindful of the pitfalls of using spectrum in certain areas.

Game theory is a way for us to analyze cognitive radio systems. You can postulate different etiquettes [such as power output] and see what happens, and then iterate upon the etiquette such that you do have a positive outcome—one that is efficient, fair, stable and predictable [for all radios in the locality]. It can be used for looking at performance issues of ad hoc networks, but it's broader than that.

EET: What else are you working on?**Reed:** Collaborative radios that work together for a common purpose. For example, I make a 911 call, and I'm inside. Can the other handsets in this region work together to help find me?

Can radios work together to fill in coverage holes, either through relaying or coordinated transmission—almost like a distributed MIMO effect? The question is how you coordinate these. [Virginia Tech has a grant] from Cisco to help us in this area, to be able to use [802.11] access points that work together for a common purpose.

EET: What will the future hold, 10 to 15 years out?**Reed:** This is one of the fun parts of the job, to be able to dream. I see smart antennas—including MIMO—becoming commonplace; with 802.11n and 3G now having hooks into smart antennas and everyone and his brother working on them in the labs for 802.16 [the IEEE standard on which the WiMax interoperability specification will be based], I think they're here. I think we'll see cognitive systems; our phones will be aware of the environment around them and

'Long-term R&D is diminishing, and I think that's disturbing for us as a nation.'

look for the best way to make a call. And there's even some talk about an "eBay" for phone calls, where carriers have to compete for your call. But the operators don't like that idea.

Also, I think [802.]16 will be incredibly disruptive.

EET: What do you dislike among the trends in the industry?**Reed:** Long-term research and development is diminishing, and I think that's disturbing for us as a nation. This trend is occurring across both industry and government. I don't think the research projects that are being funded are as revolutionary as they were in the past:

they're safer. There are no more "moon shots" out there.

EET: That's a reflection of the times, isn't it, given shrinking budgets?**Reed:** I think that's it. For instance, with the NSF [National Science Foundation], many programs have a 1-in-10 or 1-in-20 chance of getting awarded funding for that proposal. And when you look at so many, how do you eliminate programs? You look for the negative, not the positive.

And good far-reaching research will have holes in it. It will be controversial; not everyone is going to like it.

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News

PRAM, FeRAM advances displayed ...

By David Lammers

Kyoto, Japan — Researchers from Samsung Electronics Co. Ltd. (Seoul, South Korea) claimed several important advances in phase-change and ferroelectric random access memories in presentations at the 2005 Symposium on VLSI Technology here last week.

Enthusiasm for phase-change memories has waxed and waned over the past few years, with Intel Corp. admitting to difficulties in scaling its phase-change RAM (PRAM) past the 4-Mbit test stage due to various process and materials challenges. STMicroelectronics, an enthusiastic PRAM proponent, is continuing to work on the technology in cooperation with Philips Semiconductors. To date, however, the promise that chalcogenide phase-change materials would move from the world of optical disks to semiconductor memories has not been realized, said Sreedhar Natarajan, president of Emerging Memory Technologies Inc., a memory design company based in Ottawa.

Samsung's process and memory development skills could change that, Natarajan acknowledged.

Ki-Nam Kim, a Samsung senior vice president in charge of advanced memory development, said data stored in PRAMs

can be read quickly, in 15 to 30 nanoseconds. However, write times thus far have lagged, ranging from 200 ns to 1 millisecond, and write currents have been too large. Shrinking the PRAM cell size involves reducing the write current required to reset the amorphous state of the material to a crystalline state.

Researchers detail FeRAM, phase-change architectures.

It is thermal energy that induces the phase change from the amorphous to the crystalline state. Achieving a smaller write current depends on creating efficient bottom electrode contacts (BECs) to transfer heat to the bit cell.

At the symposium, Samsung senior engineer Su Jin Ahn described the company's plan to develop a standalone 256-Mbit phase-change RAM over the next year or so, using a 0.10-micron process to achieve a cell size of 0.16 square micron.

The Samsung team focused on the

BEC design and fabrication, designing a ring-shaped contact to replace the conventional solid pillar-type contact. The ring has the same patterned area but the physical area of contact is smaller than the plug-type contacts, which supports the goal of a reduced write current. Kim said that the new design has a write current of 0.4 milliamperes.

Kim said Samsung expects to develop a commercially available PRAM product "within a couple of years, taking some part of the NOR flash market."

Samsung senior engineer D.C. Yoo described a metal oxide chemical vapor deposition process that creates a much improved interface between the ferroelectric material and the bottom electrode, made of layers of iridium and an SRO alloy composed of strontium, ruthenium and oxygen.

"In the past, 50-nm PZT capacitors have shown poor reliability," Yoo acknowledged. But the improved deposition method and the switch to SRO for the bottom electrode have resolved the reliability issues, he said.

With an additional six mask layers, the FeRAM array can be embedded into a logic process for products such as smart cards, he said.

As MRAMs shift paths at VLSI forum

By Yoshiko Hara

Kyoto, Japan — Long considered a potential next-generation memory, magnetoresistive RAM was in the spotlight at last week's VLSI symposium.

Fujitsu Laboratories Ltd. and the team of NEC Corp. and Toshiba Corp. presented new approaches to MRAM circuitry and cell structure, respectively. The companies said they were establishing essential technologies for MRAMs, which are nonvolatile, blessed with unlimited read/write cycles and expected to enter practical widespread use around 2008.

NEC and Toshiba formed a joint R&D MRAM project in 2002. At last week's symposium, the team proposed a toggle-mode MRAM cell. Its magnetic tunnel junction with a multilayered structure, the team said, solves the toggle-switching issue.

"With this multilayer toggle-mode cell, the programming margin becomes large and switching current can be lowered. The structure is suitable for large-scale integration," said Shuichi Tahara, chief research manager of NEC's System Devices Research Laboratories.

"Lower current operation is essential for scaling down," said Hiroshi Yoda, chief specialist at the advanced-memory unit of Toshiba's system-on-chip research and development center.

The NEC/Toshiba team introduced a four-layered structure that allows MRAM

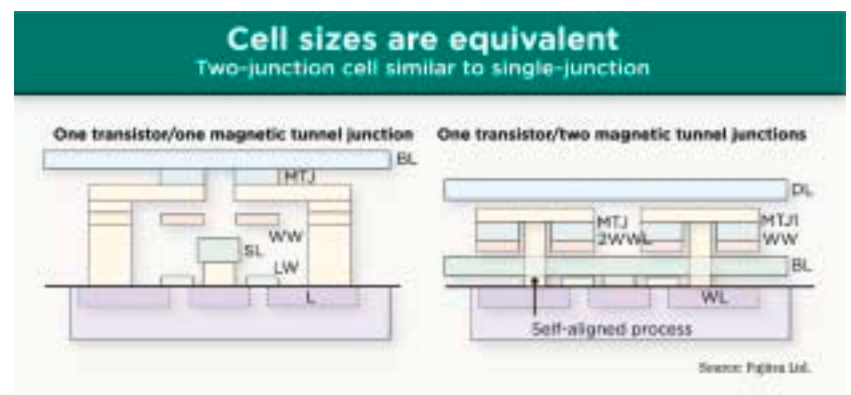
threshold and saturation levels to be controlled independently.

The 50-researcher team, evenly drawn from Toshiba and NEC, aims to develop a prototype 256-Mbit device using a 250-nanometer magnetic tunnel

junction and 130-nm CMOS by March 2006. The companies are discussing a possible second phase of the project.

MTJs were connected in series. Fujitsu fabricated the test device with each MTJ measuring 0.2 x 0.4 micron and confirmed the cell operation.

"The hurdle of integrating MRAM is high, especially for large-scale integra-



tion, and the margin is getting narrower," said Hitoshi Tanaka, director of Fujitsu Labs' Silicon Device Laboratory. "Our approach is to come up with a new idea in circuit design to secure a wide margin."

DRAM-like architecture

Separately, Fujitsu is developing embedded MRAM to differentiate its system-on-chip products. Its Fujitsu Laboratories unit has proposed a one-transistor/two-magnetic tunnel junction (1T/2MTJ) structure MRAM cell with a direct voltage-sensing scheme, which it said has the advantages of DRAMs.

In the proposed 1T/2MTJ cell, two

The voltage sensing enables a folded bit-line layout and a burst-mode operation for high-speed readout, which are widely used technologies in DRAMs, said Masaki Aoki, senior researcher at the Silicon Device Lab. "Using the same kind of sense amplifiers, the 1T/2MTJ MRAM will have a high efficiency of space usage like DRAM," said Aoki.

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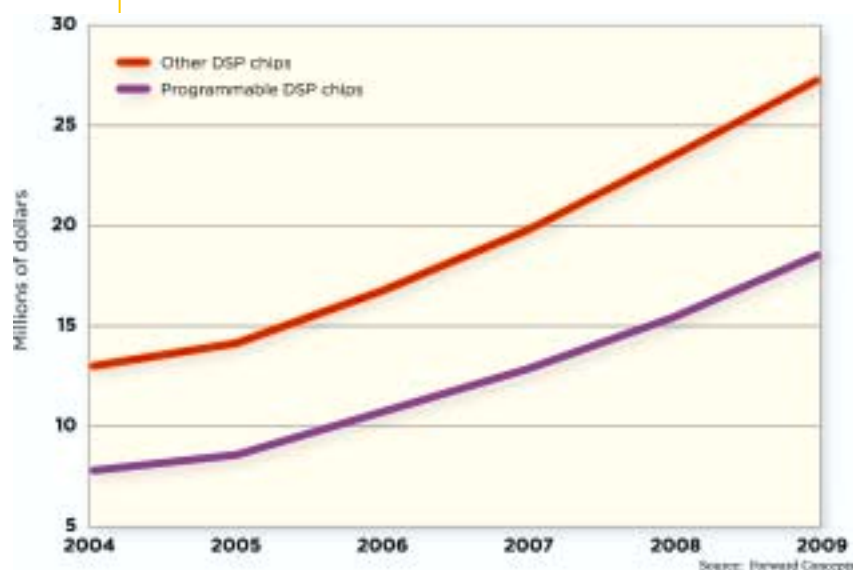
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By the Numbers

DSPs send positive signals



Programmable digital signal processors, which composed 37.5 percent of the DSP chip market last year, will show an 18.9 percent compound annual growth rate through 2009; all other DSPs will attain a 15.9 percent CAGR, said Forward Concepts (Tempe, Ariz.). Fixed-point devices made up 97 percent of 2004 shipments and floating-point 3 percent. A handful of vendors dominate this sector.

2004 market shares

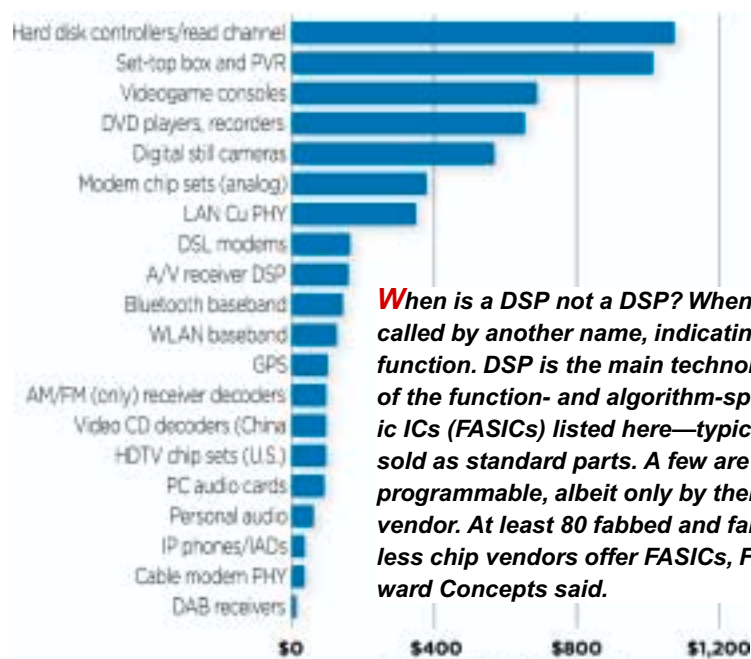


Overfed Americans?

Programmable DSP shipments by region, 1Q2005



Cellular subscriber applications made up 67 percent of the programmable DSP market in 2004, with most expansion overseas. China is the biggest cell market in the world, said Forward Concepts.



When is a DSP not a DSP? When it's called by another name, indicating its function. DSP is the main technology of the function- and algorithm-specific ICs (FASICs) listed here—typically sold as standard parts. A few are programmable, albeit only by their vendor. At least 80 fabbed and fab-less chip vendors offer FASICs, Forward Concepts said.

Riding the learning curve



Even as the speed, functionality and on-board memory of programmable DSPs have grown significantly over the years, "high-volume manufacturing, the relentless migration to smaller [process] geometries and competitive price pressures" have pushed prices ever lower, said Forward Concepts president Will Strauss.

DSP chip market

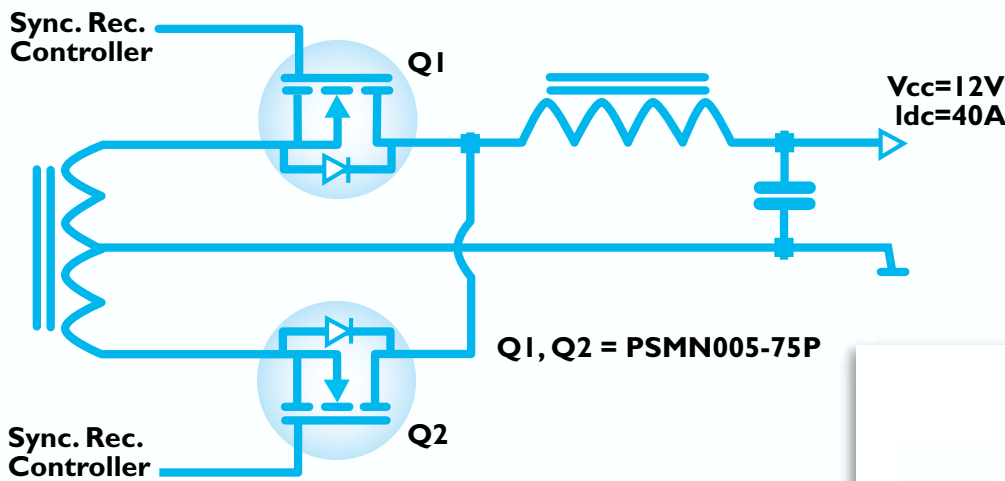


—Compiled and written by David Roman



V _{DS} (V)	R _{DS(on)} (max) @ 10V (mΩ)	I _D (A)	DPAK (SOT428)	D ² PAK (SOT404)	TO220AB (SOT78)
75	8.5	75		PSMN008-75B	PSMN008-75P
75	5.0	75		PSMN005-75B	PSMN005-75P
100	8.8	75		PSMN009-100B	PSMN009-100P
100	25.0	47	PSMN025-100D		
100	15.0	75		PSMN015-100B	
110	15.0	75			PSMN015-110P
150	30.0	55		PSMN030-150B	PSMN030-150P
150	63.0	29	PSMN063-150D		
200	57.0	39		PSMN057-200B	PSMN057-200P
200	130.0	20	PSMN130-200D		

Secondary Side Synchronous Rectification



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Immortal Works

All hail our June caption writers, who have managed to please our fastidious, curmudgeonly judges to gain instant fame. Their clever words follow.



"SONG ENGINE," BY RAYMOND SWANLAND, FROM ODDWORLD STRANGER'S WRATH VIDEOGAME

June winning caption

"Quick, launch the debugger."

Team EETnet: Don Swaab, Senior Engineer, Swaab Consulting, Maple Shade, N.J.; Jim Randazzo, Senior Engineer, JJR and Associates, Lebanon, Mo.

NASA specs out the grasshopper.

Robb Cole
Electrical Engineer Staff
Lockheed Martin Systems
Integration
Owego, N.Y.

Thrinx from Bberflxl was surprised to find a female on this planet but was nonetheless frustrated in his attempts to mate with a microwave tower.

Stu Bell
Senior Software Engineer
DPHI Inc.
Boulder, Colo.

"I asked for Tiny Bubbles and they sent Big Noise From Winnetka."

Warren Podolske
Director
Milwaukee Metal Products
Co.
Milwaukee

"OK, OK, I'm sorry I accused you of a Bushism when you told me there was a bug on our hardware."

Terry Smith
Electrical Design Engineer
Ryko Manufacturing Co.
Grimes, Iowa

"Man, have we got a bug!"

Jack Chernega
Project Engineer
EMF Systems Inc.
State College, Pa.

First extraterrestrial Intel fab blatantly violates Craig Barrett's "copy exactly" strategy.

Will Arthur
Senior Software Engineer
Intel Corp.
Columbia, S.C.

"I built this when my neighbor bought his son a set of drums."

Steven L. Comee
Engineer/Scientist
The Boeing Co.
Canoga Park, Calif.

As we approached the customer's main office, we sensed that there would be a few technical challenges ahead.

Bill Norr
Lead Communications
Engineer
The MITRE Corp.
Mount Arlington, N.J.

"Trick or treat!"

Gary Mason
Software Engineer
LML
San Jose, Calif.

"Do we have to take this trip every time to talk to the thermal guru?"

Chris Wyland
Manager
Philips Semiconductors
San Jose, Calif.

"It always happens: You slay every dragon, climb over impossible obstacles and then, bingo, right as the goal is within reach, management swoops in and takes all the credit."

Michael T. Wright
Technical Staff Engineer
General Dynamics
C4 Systems
Scottsdale, Ariz.

"Oh, shit! One of our engineers has been drinking again."

E. Ralph Egloff
President
Egloff Associates
Skokie, Ill.

"... and off to our left, the largest, nastiest system bug our company ever had to deal with."

John Muren
Staff Electrical Engineer
Encad Inc.
San Diego

"Play Misty for me."

Simon Robbie
Senior Software Engineer
Quark Inc.
Denver

"I think engineering overdesigned the new 3-D HDTV."

Gary Mason
Software Engineer
LML
San Jose, Calif.

"You think that's bad, last night I had a nightmare that I was stuffed into an 8- x 9-foot cubicle strapped to an ergo chair irradiated by neon lights and CRT tubes while surrounded by hundreds of others with the same plight."

Mark Klemkosky
Staff Engineer
Intel Corp.
Chandler, Ariz.

As the engineering team came back from lunch 15 minutes late, they could not help but wonder if this attracted the attention of their autocratic manager, who was waiting for an opportunity to discuss the monthly productivity numbers.

Kevin Parmenter
FAE Director
Fairchild Semiconductor
Gilbert, Ariz.

Human droids make the long and arduous climb to offer monetary sacrifices in attempts to appease the Microsoft god for a virus-free season.

Ron Kyker
Wireless and Embedded
Systems Engineer
Sandia National Labs
Livermore, Calif.

"I started out building a continuous flow teapot, but I couldn't help adding bells and whistles."

Steven L. Comee
Engineer/Scientist
The Boeing Co.
Canoga Park, Calif.

"Hey, boss, I had a dream last night after you told me that we would be climbing the management ladder as soon as you had outsourced our engineering department!"

Jackson Leung,
Member of Technical Staff
Nanya Technology Corp.
Houston

"Going to these project phase gate reviews with upper management makes my heart beat faster! Look at the A/V equipment in that conference room!"

Ken Whiteleather
Senior EE
Sparton Medical Solutions
DeLeon Sprgs., Fla.

"Get peddling, dude, you're going to topple over the edge."

Simon Robbie
Senior Software Engineer
Quark Inc.
Denver

The more trivial the announcement, the bigger the hoopla.

Michael T. Wright
Technical Staff Engineer
General Dynamics
C4 Systems
Scottsdale, Ariz.

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COMPANIES

Up and Comers on the Leading Edge

TO WATCH

Tanner EDA: Finding Ways to Alleviate Design Headaches

Software provider's cost-effective and easy-to-use tools help



UP and-Comer
At-a-Glance

Tanner EDA

Headquarters:

Pasadena, Calif.

Line of business:

EDA tools aimed at improving IC and MEMS design, layout and verification processes

No. of employees: 75

Key products:

HiPer Verify design rule-checking software; L-Edit layout and verification tool, and T-Spice Pro analog/mixed signal design solution

Top customers:

- Catalyst Semiconductor Inc.
- CSR plc
- Honeywell International Inc.
- Jet Propulsion Laboratory
- Linear Technology Corp.
- NEC Corp.
- Sarnoff Corp.
- Semiconductor Technology Associates Inc.
- Ricoh Company Ltd.
- Xerox Corp.

Why to watch:

Tanner EDA tools are efficient, enable innovation and support rapid development cycles

Even before Dr. John Tanner graduated from the California Institute of Technology 17 years ago, he co-founded a company that designed integrated circuits and quickly discovered that existing tools were expensive and difficult to work with. He also found that creating layout, verifying its correctness and simulating circuits were time-consuming and awkward processes.

Determined to find a better solution, Tanner set out to create a software platform that would be cost-effective, easy to use and flexible enough to handle even the most complex design processes.

That philosophy remains the driving force behind Tanner EDA today.

The Pasadena, Calif.-based company, now on its 11th release of its original software, has developed a breadth of tools geared to improving the design process, reducing design cycle times, increasing productivity and reaching time-to-market goals.

"If we fast-forward 17 years, you'll see a worldwide company that is still true to its roots and cares about the needs of its customers," says Daniel Hamon, Tanner EDA general manager.

Building on Its Heritage

Determining the needs of its customers – engineers hailing from the aerospace, biomimetics, electronics, industrial and medical industries – has long been a fundamental principle for Tanner EDA. To keep a pulse on what customers want, Tanner EDA has stacked its staff with engineers and industry experts who have firsthand knowledge of how the design process works and understand the pain points that come with it.

"The tools are designed with a great deal of input from designers who know what customers need from the user interface," adds Hamon.

Besides having industry know-how embedded in the software development process, Tanner EDA also strives to offer value-priced solutions that can be easily implemented by start-ups, mid-size and multi-million dollar top-tier players.

On that front, Tanner EDA tools run on the Windows platform and tackle a range of design issues, including design capture, layout, tapeout and verification. The software, which has been used by customers designing innovative components for Bluetooth capabilities, the Mars Rover space

program and advanced medical devices, is also compatible with other back-end EDA systems and import and export industry-standard formats like GDS, CIF and DXF. Another advantage: These user-friendly tools can be installed and integrated into the design process quickly.

We believe that tools are meant to help the design process. They are not meant to be an obstacle in getting a product to silicon.

— Daniel Hamon, Tanner EDA general manager

"The beauty of the tool is that it is incredibly flexible," says Dr. Massimo Sivilotti, Tanner EDA chief technology officer. "We have architected the tools so they are easy to use and easy to configure."

And, that's what engineers are looking for – more powerful tools that they don't have to fumble with but, at the same time, can handle complex design flows. In turn, an easier-to-use solution brings with it increased productivity and shortened design cycles, which are things that impact overall operations, revenues and profits.

"If you are a start-up or have a limited budget or tight time-to-market goals, you can't afford to spend a great deal of time or money building your infrastructure," says Dr. Sivilotti. "You need to be able to work in the most efficient way."

Take Your Pick

With engineering efficiency in mind, Tanner EDA, which has issued 25,000 licenses for its software products, has developed a suite of tools to help customers achieve that goal.

Its L-Edit series, for example, handles layout and verification processes for analog, mixed-signal and MEMS products. Meanwhile, Tanner EDA's HiPer Verify provides foundry-compatible design rule checking that meets submicron DRC requirements. And, T-Spice Pro gives designers the ability to do table-based modeling for simulations.

"We believe that tools are meant to help the design process," Hamon says. "They are not meant to be an obstacle in getting a product to silicon."

For more information go to www.tannereda.com or call 1-877-325-2223



Building Blocks

VERIFICATION

Tool buffs up regression testing

By Richard Goering

Anaheim, Calif. — A verification management tool that can help speed IC regression testing made its debut at last week's Design Automation Conference here. Called Advanced Verification System (AVS), the tool is the first software offering from value-added reseller TeamEDA Inc.

AVS provides a browser interface that serves as a control panel for the verification process, where jobs can be launched, suspended or terminated. It organizes and runs tests, provides various types of reports, and can halt the simulation and inform users of any problems.

Launched about a year ago, TeamEDA resells Opteron and Linux servers from Rackable Systems, the load-sharing facility (LSF) job-queuing and load-balancing software from Platform Computing Inc., and reporting software from Open iT Inc. It also provides consulting services. But the company's main mission is to be a software developer, said Guy Haas, TeamEDA president.

AVS was developed by design consultant Scott Nogueira, who has a 20-year history in EDA tool development. After working for in-house CAD groups at Digital Equipment and Sun Microsystems, he became a consultant, and that's where the idea for AVS was born.

"AVS is based on my experience of doing this kind of work frequently at various sites I've gone to," Nogueira



said. "I've developed it 10 times over for my customer sites, but there's nothing really like it in the market out there."

Haas said AVS 1.0 is now used with two customers, Enterasys Networks Inc. and TranSwitch Corp. It's ready to use with the concurrent-versions system (CVS) file management system, Modelsim simulator and LSF, he said. TeamEDA's intent is to add support for Clearcase and Perforce for file management, Sun grid engine for job queuing and other simulators like Synopsys VCS and Cadence NC-Sim.

"Basically, we're taking the execution of your verification suite, helping you organize those tests, firing them off to a batch environment, monitoring the results and notifying you of the results of your simulation," Nogueira said. "The idea is to make engineers more productive in the regression environment." Nogueira said AVS also supports "best practices," such as

setting up new CVS working directories for regression runs and making sure that simulation models compile properly.

Much of what AVS does is handled today by in-house scripts, Nogueira said. But, he said, those scripts are not as robust or as functional as the AVS package. "Companies also don't want engineers to spend time home-baking these things," he said.

CONTINUED ON PAGE 38

VIDEO

\$20 IPTV chip boosts speed, uses less power

By Rick Merritt

Campbell, Calif. — Equator Technologies Inc. launched a fifth generation of its video processor today for emerging markets like Internet Protocol TV set-top boxes and digital media adapters. The relatively low-cost BSP-16 arrives as the company merges with Pixelworks Inc., a fast-rising maker of display chips.

"With these two moves, the competitive situation between us and the big DSP players has significantly shifted," said John O'Donnell, chief technology officer of Equator.

In the past, Equator lacked a \$20 part to compete with general-purpose DSPs from companies like Analog Devices and Texas Instruments, which also have significantly larger sales and support staffs. With the acquisition, 75-person Equator teams up with Pixelworks (Tualatin, Ore.), which boasts 350 employees, roughly a third of them in the booming China market.

Before the merger, Equator had only two of its five sales and support staff focused on China, where the company spent 18 months working on emerging IPTV networks. For Pixelworks, the merger with Equator buys it a fast entry into the nascent IPTV business and a programmable video processor to replace a hardwired device in its portfolio that it OEM-ed from an unnamed chip supplier.

CONTINUED ON PAGE 42

POWER MANAGEMENT

Converters move on-chip to regulate SoC's voltage

By Ron Wilson

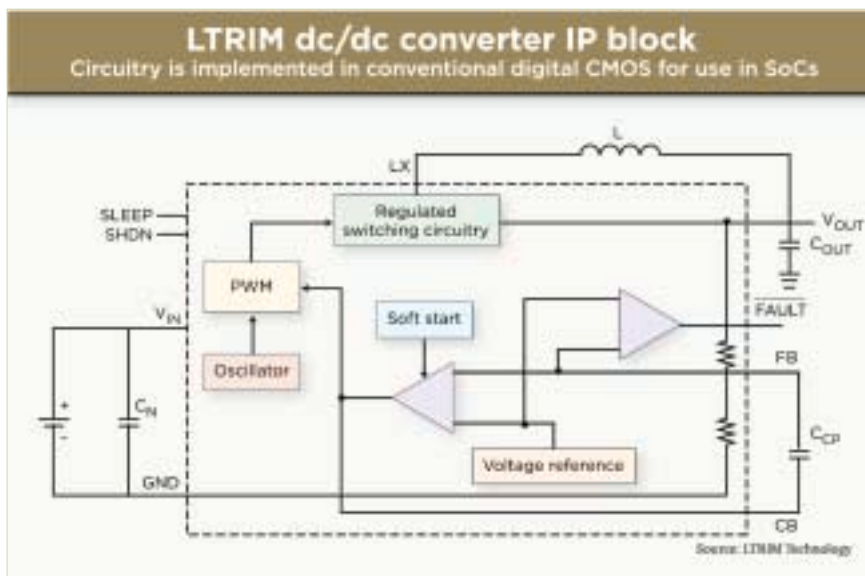
Fremont, Calif. — While most of the attention in system-on-chip design remains focused on digital issues—IP selection, interconnect architecture, memory generation and the like—yet another kind of integration problem is quietly creeping up on designers, especially in compact, highly mobile applications. This one involves power—not power reduction, but power supply.

"Miniaturization is forcing system designers of very compact devices, like MP3 players, to consider moving voltage regulation onto the SoC," argued Mike Shamshirian, vice president of sales and business development at LTRIM Technology. "Not only is there no room left in the package for an external voltage regulator or dc/dc converter, but SoCs increasingly require multiple voltages.

That increases the number of supply and ground pins and the susceptibility to noise coupling onto the those pins."

Other, more challenging issues are coming up as well. As designers increasingly turn to voltage islands and dynamic voltage/frequency scaling to reduce power consumption, the power needs of particular blocks on the SoC are becoming quite dynamic—so much so that it is a challenge to package and chip-routing resources to deliver rapid changes in current and voltage from an external pin to the block. This may force designers to integrate point-of-use regulators onto the die for some blocks. In addition, die-to-die process variations might require tuning the voltage to the characteristics of a particular die, maybe even at a particular operating temperature.

CONTINUED ON PAGE 44



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TOSHIBA

Building Blocks

DESIGN TOOLS

Virtual system 'platform' rolls

By Richard Goering

Anaheim, Calif. — Making the move from point tools to a more integrated platform, Carbon Design Systems Inc. rolled out its Virtual System Prototyping (VSP) product here at last week's Design Automation Conference. It promises to run billions of simulation cycles in a matter of hours, enabling both hardware and software validation.

Carbon launched its SpeedCompiler and DesignPlayer tools in December 2003. These tools generated fast cycle-accurate models derived from RTL code.

They produced linkable object representation with a C-language API, creating a model that runs 50 to 200 times faster than event-driven simulation.

Now, Carbon is taking that compilation technology and creating a more complete solution, said Alan Swahn, vice president of marketing at Carbon. The new VSP solution replaces SpeedCompiler and DesignPlayer, which were "point tools," Swahn said.

The earlier tools "generated a C object, but the user had to do something with it," Swahn said. "They had to put it in their own environments and sometimes build transactors. It was essentially a build-your-own system. The difference with VSP is that we have a platform that makes it very easy for them to build their prototype."

Most other fast validation solutions, Swahn said, either don't have the same performance or they require hardware. VSP is purely a software solution.

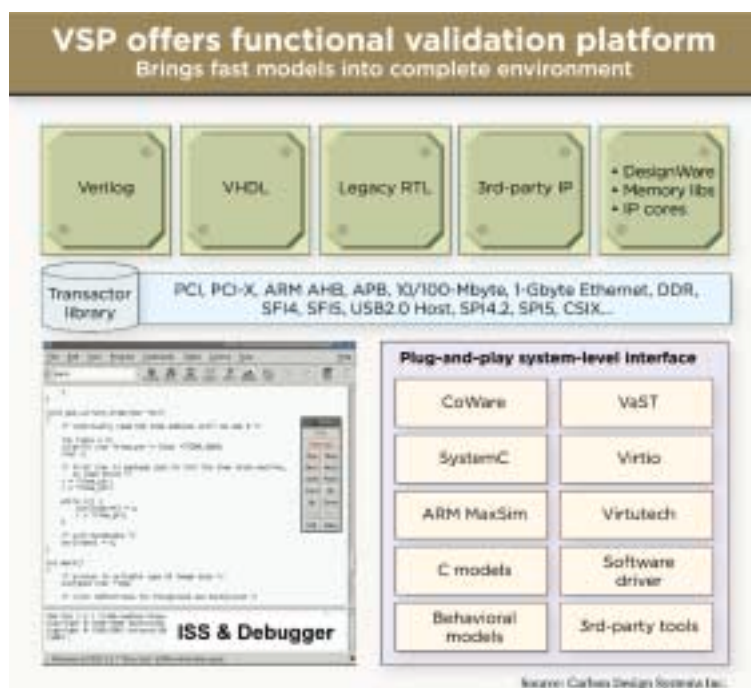
The offering can be used by software developers to get a jump on code development and debugging, as well as hardware designers who want faster verification.

Much of what's in the VSP platform stems from partnerships. It includes verification transactors

resold through an OEM agreement with Zaiq Technologies Inc.

These transactors provide a "bridge" between instruction-set or transaction-level models and more-detailed models that work at the pin level. They're available for many common communications protocols, such as PCI, PCI-X, ARM AHB, Ethernet, DDR or USB.

VSP doesn't come with processor models, but it provides integration with ARM's MaxSim instruction set simulator, which was demonstrated by



both Carbon and ARM at DAC. It also offers interfaces to other providers of fast processor models and virtual prototyping solutions, such as Vast Technologies, Virtio and Virtutech.

Carbon intends to provide silicon intellectual property libraries with VSP, but the IP core library isn't ready yet. The product does come with a memory library and an ability to "remodel" the elements in Synopsys' DesignWare library to run faster, Swahn said.

VSP will ship July 1 with prices starting at \$35,000 for a one-year license.

SILICON PROCESSING

Process engineers passing the buck to designers over low-k

By Ron Wilson

Burlingame, Calif. — Papers and panels at the recent International Interconnect Technology Conference here showed growing fissures in the once-solid compact between the back-end-of-line (BEOL) process engineers who create the interconnect stacks in ICs and the chip designers who use them. In the past, as interconnect geometries have shrunk, process engineers have selected new materials and invented techniques to ensure chip designers would have viable metal resistance and intermetal capacitance with which to do their work. But beginning at the 65-nanometer node, BEOL engineers are retreating as the interconnect integration task goes from hard to Herculean. That leaves chip designers tapping their own resources to use the interconnect characteristics they are given.

IITC papers reflected "a slowdown" in the International Technology Roadmap for Semiconductors, said Cindy Goldberg, distinguished member of the technical staff at Freescale Semiconductor's Crolles, France, labs. "Engineers are reporting very conservative choices in materials for the 65-nm node and beyond. There is a definite shift of the burden of innovation from process engineering to the circuit designers."

Standing pat

That has led some companies not to change materials from 90 to 65 nm. IBM Microelectronics, with its new Cu65 process, chose to stay close to the same stack that worked at 90 nm, said vice president of semiconductor products Tom Reeves. IBM has increased transistor drive current with strained channels and by bringing its internal statistical-timing tools into the public tool chain.

Even so, IBM sees 65 nm initially as limited in raw performance by the behavior of the conservatively designed interconnect stack. "We will have about a 20 percent improvement in transistor performance," Reeves said. "But it is increasingly difficult to extract system-level performance from that. Initially, we will be exploiting the density rather than the raw speed of 65 nm in our ASIC process."

Freescale will have two versions of its 65-nm process, Goldberg said. "The first is just an extension of our 90-nm technology." The second will use porous low-k materials to get better capacitance, but at a higher die cost and with more-

CONTINUED ON PAGE 44



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Building Blocks

SILICON PROCESSING

Team refines dual liners for 65-nm SOI process

By David Lammers

Kyoto, Japan — A team based at IBM's Hopewell Junction, N.Y., silicon development center came to the Symposium on VLSI Technology here last week to detail its 65-nm silicon-on-insulator platform. The development team includes Advanced Micro Devices, IBM, Sony and Toshiba.

Advanced Micro Devices Inc., for one, expects to qualify the SOI process at its Fab 36 in Dresden, Germany, by the end of the year, moving to commercial production next year, said Nick Kepler, vice president of logic development at AMD.

Performance improvement at the 65-nm node relies largely on enhancement of

the dual-stress-liner approach, first described by the partners at the International Electron Devices Meeting last December. Given the present lack of a high-k gate oxide, the team left the nitrided gate-oxide thickness for the 65-nm transistors roughly the same as the previous node, at 1.05 nm. With the same gate-oxide thickness,

voltage also was left intact: the transistors can be operated at greater than 1 volt with 10-year reliability for high-performance applications, or can be driven at less than 1 V for mobile processors.

Kepler said that the 35-nm gate length also was not changed much from the previous node, given concerns over short-channel effects.

That leaves strained silicon as the main knob to turn. Kepler said AMD brought the dual-stress-liner approach into its 90-nm products, and last year retrofitted it into some 130-nm-based chips to gain a relatively pain-free performance enhancement. The SOI team enhanced the DSL approach for the 65-nm node.

Intel Corp. uses a nitride liner on the NFET transistors to induce a tensile stress and deposits silicon germanium at the source and drain regions of the PFET to create a compressive stress.

Kepler said, "Intel didn't think dual liners were manufacturable. We thought it was more manufacturable than adding SiGe. Both IBM and AMD folded the dual-stress liners into our 90-nm products and didn't miss a beat in terms of yields."

For the 65-nm process, the team optimized the liner approach in various ways. As the transistors get smaller, the same-thickness nitride-capping layer exerts a proportionately bigger strain.

Nickel as the silicide metal, rather than cobalt, was the one new process module introduced for the 65-nm node.

Verification tool

FROM PAGE 34

AVS 1.0's browser GUI can monitor jobs remotely. It organizes a "test matrix," which defines all the user's tests and how they run. It initiates the compile process for simulation models, runs simulations and monitors results. If there's a showstopper during a long regression run, like a compiler error, it can call or e-mail the user.

Nogueira said AVS produces "great graphical and tabular reports that have hypertext links." There are real-time session status reports, which tell how the session is going, and historical session reports, which provide session and test data after simulation is completed. Reporting can include code coverage results.

Haas said that TeamEDA will start shipping AVS around the end of this month. The company plans to ship the software preloaded onto a Dell SC420 server. TeamEDA can also install it on the customer's server. An annual subscription license is \$12,500, including support.

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SILICON ENGINEERING

Low-temperature adhesives putting heat on solder

By R. Colin Johnson

Portland, Ore. — Low-temperature, low-profile conductive adhesives are poised to enable ultraflat-panel displays for cell phones, laptop computers and wall-mounted televisions.

Going beyond recommendations to take the lead out of solder, researchers at the Georgia Institute of Technology are working to build a world of electronics free of metal-solder itself.

While the interconnect trade association IPC and other organizations are pursuing a no-lead goal, they “are only looking at low-temperature adhesives as one of many different alternatives,” said Ching-Ping Wong, professor of materials science and engineering at Georgia Tech (Atlanta). “We believe that our approach to low-temperature adhesives has much greater potential because we are solving the fundamental problems that make others hesitant to use them.”

Other approaches to low-temperature conductive adhesives have been afflicted with self-alignment and low-carrier mobility problems. Wong’s group, which included graduate student Grace Yi Li and post-doctoral researcher Kyoung-sik Moon, is working to overcome those obstacles.

Lead-based solder has traditionally been used to affix components to printed-circuit boards, but IPC and other industry organizations have been encouraging a switch from lead to tin alloys, which don’t pose the same danger or hazard. In addition, the European Union’s Restriction of Hazardous Substances

directive will limit the lead in electrical equipment sold in Europe after July 1, 2006.

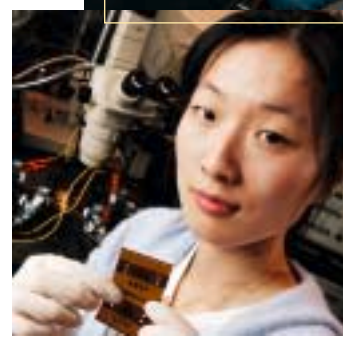
The IPC road map (<http://lead-free.ipc.org>) calls for adding alternative metals as nanoparticles into tin-alloy solder. However, the Georgia Tech researchers propose going straight to electrically conductive adhesives using a metal powder filler, such as silver, that conducts electricity inside a polymer resin. Wong said that these resins—essentially an epoxy of silicon or polyimide—offer greater adhesion, mechanical strength and affect resistance.

Low-temperature conductive polymers also hold an edge over tin alloys, which melt at higher temperatures than lead, lowering the yields of today’s lead-free pc boards. Some components are particularly sensitive to heat, so manufacturers are reluctant to switch materials.

“Tin alloys of silver and copper provide the best combination of strength, fatigue resistance, plasticity and reliability, but they still tend to have a higher melting point than lead, thus subjecting the board and CMOS components to higher stress,”



Ching-Ping Wong works with grad student Grace Li Yi. At left, she holds low-temp adhesive.



said Wong. “Gallium arsenide chips are especially sensitive to temperature, making them prime candidates for our low-temperature adhesives.”

Wong cited other

advantages:

- Tin alloys of silver and copper have a melting point of 217°C, or 34° higher than a tin-lead alloy’s melting point of 183°C. But low-temperature adhesives can essentially be applied at room temperature, enabling low-cost, thin and flexible polymers to be used as pc-board materials.
- As an alternative to lead or tin alloys,

low-temperature adhesives allow expensive components to be assembled without risking damage from overheating.

• Low-temp adhesives are more expensive but offer a lower profile for circuit boards, adding only a few microns of thickness, perhaps 100 times thinner than metal solder. Some applications, such as cell phone displays, have bitten the bullet and switched to low-temp adhesives despite their higher cost.

“Besides being lead-free, our adhesives are applied at a lower temperature than lead, plus they provide a lower profile—adding only a few microns to the thickness of a printed-circuit board

whereas metal solder adds over 100 microns,” said Wong. “This helps make LCD displays for televisions, laptop computers and cell-phones much thinner.”

But low-temp adhesives cannot be used in high-current applications today because of the inherently lower carrier mobility of conductive adhesives compared with metal solder. Also, because solder is not sticky, many of the assembly methods used today rely on self-aligning components, whereas adhesives require pick-and-place equipment to be much more accurate. Wong’s team at Georgia Tech said it’s solving these problems, potentially making low-temperature conductive adhesives applicable for all phases of electronic assembly.

NETWORK INTERFACES

Switches, cards support both Ethernet and Myrinet

By Loring Wirbel

Colorado Springs, Colo. — Myricom Inc., developer of the widely used Myrinet in high-performance computing applications, will introduce “bilingual” 10-Gigabit network interface cards and system-level switches this week that use both Ethernet and Myrinet protocols.

But moving in behind Myricom is a newcomer that will take on iWarp, Infiniband and TCP offload engine concepts for accelerating Ethernet. Level 5 Networks Inc. claims that by duplicating TCP stacks in the user space, it can offer channel performance comparable to Myrinet or Infiniband while preserving all native Ethernet protocols.

Myricom will introduce its new generation at the 2005 International Supercomputer Conference in Heidelberg, Germany, this week, because of the network’s traditional base in high-performance computing. Level 5, by contrast, is aiming at the data center, with grid and supercomputing as secondary markets. In both realms, first-

generation high-speed networks and fabrics initially were seen as threatened by PCI Express Advanced Switching and Serial RapidIO. With several new concepts for accelerating Ethernet performance, however, Ethernet’s future as a backplane and fabric looks more promising.

While many in the serial-interconnect community worry about the ubiquity of Ethernet Layer 2 framing, Myricom founder and president Chuck Seitz said it’s not so much the protocol as the price points of 1-Gigabit and 10-Gigabit Ethernet that spurred Myricom to make a response.

Myrinet has become well-established in such supercomputing environments as national energy labs, automotive development and oil exploration. While Infiniband temporarily threatened to take market share in the grid-computing cluster world, its limited acceptance kept

Myrinet alive and well. Indeed, many companies in the Infiniband community have turned to iWarp and remote direct memory access (RDMA) as Ethernet-based alternatives to Infiniband.

Myrinet has moved from being

proprietary to being a full ANSI standard, implemented on such operating systems as Linux, Mac OS X, Windows, Solaris and FreeBSD, offering Ethernet emulation through TCP/IP. The Myrinet network interface cards (NICs) were designed from the

beginning as firmware-powered offload engines. Moving to an Ethernet interface does not take away such advantages of the Myrinet environment as multipath routing and OS bypass.

The Myri-10G switches, expandable from 16 to 128 ports, will be priced as low as \$400 per port, depending on configuration. The PCI Express NICs, popu-

lated with 10GBase-CX4 interfaces, will list at \$795. The cards offer offloads for Internet Protocol checksum operations and full OS bypass. The Myri-10G NICs carry the advantage of being able to be used with any 10-Gigabit physical-layer device. The NICs and switches scale in the same way as Myrinet 2000 and offer full routing at Layer 2.

Level 5’s method of improving stack performance is dubbed EtherFabric and is significantly different than the iWarp and RDMA development efforts that grew out of Infiniband, said Dan Karr, chief executive of the U.S. Level 5 operation in Sunnyvale, Calif.

The EtherFabric NIC is fully compatible with both TCP/IP and Sockets, requiring no porting or recompiling of applications. The current 1-Gigabit Ethernet card, offered in both PCI and PCI-X versions, will be followed by 10-Gigabit versions. In the meantime, Level 5 will offer a dual-port 1-Gigabit/port host bus adapter card for \$495, in general availability this month.

Myricom,
Level 5
place their
bets.

Building Blocks

COMMUNICATIONS TESTING

Two specialists bolster support for triple-play

By Loring Wirbel

Chicago — Test companies with a legacy in packets are beefing up video test parameters to build the best solutions for “triple play” broadband networks. Spirent Communications came to the recent Supercomm show with more than 20 point solutions for voice and video, many

centered on the Abacus test platform. Agilent Technologies Inc., meanwhile, offered updates to the Network Tester and N2X systems for R&D, as well as for the Distributed Network Analyzer Pro used in carrier network maintenance.

Mark Fishburn, vice president of technical strategy at Spirent, noted that voice

quality needs to be tested in the presence of data and video, while video needs to be tested as data and voice are simultaneously being carried on the network. “The solutions have to be modular because of the widely divergent triple-play architectures, but they all must be tested as a unified broadband delivery network,” he said.

An example would be digital subscriber line networks’ adding support for new DSL types like VDSL2, even as they carry Internet Protocol TV over DSL access multiplexers.

Internet Group Management Protocol (IGMP),” said Hitoshi Tanaka, director of Fujitsu Labs’ Silicon Device Laboratory “joins” and “leaves,” used during IPTV channel surfing, must be tested in the presence of new physical-layer chip sets for DSL. Fishburn said that when IGMP is used for fast channel surfing, quality can degrade if carriers are not prepared to handle the higher-layer protocols.

Spirent, Agilent solutions

Video quality assessments based on the International Telecommunication Union’s J.144 standard have been added to the Spirent suite through a partnership with Psytechnics (Ipswich, England).

Many of the new test solutions use the Abacus 5000 platform, since it is designed to test IP telephony systems, and many measurements for jitter and mean objective scores can be mapped to IP video performance parameters. Avalanche, a lab analyzer for advanced IPTV protocols, also is used in the bundled solutions

Spirent offers. Multidimensional tests are carried out with a new integration tool, the Converged Network Impairment Emulator, that emulates system degradation in the presence of multiple services.

Agilent Technologies is approaching both lab and field systems with a similar integrated approach.

Bill Tomeo, marketing manager for DNA solutions at Agilent, said network analyses for triple-play must extend as far as policy managers and Radius authentication servers, tying network performance

to subscriber authorization rights. In the lab, emulated problems must scale to hundreds of thousands of subscribers; in the field, testers must be able to correlate triple-play service from solutions that are either portable or embedded.

The N2X protocol analyzer supports IGMP tracking, multicast virtual private networks and other specialty IP domains found in broadband home networks. The complement to the emulating N2X, Network Tester, stresses single ports with tests of file-sharing, gaming, denial-of-service attacks, based on IP or on a proprietary protocol mix. The NT system can test IPv6 networks and offers full emulation support for SIP and H.323 voice, testing single ports that carry all three services, even under conditions of external attack.

In the field, Agilent’s DNA Pro not only handles IP and Ethernet protocols but also brings in wireless traffic through support of HSDPA and UMTS protocols. Test configurations vary from remote unattended units to active dispatched on-site testing.

Video chip

FROM PAGE 34

“The BSP-16 is all about cost, schedule and power dissipation,” O’Donnell said. The \$20 part, sampling now, integrates such functions as an IDE hard disk and NAND flash controllers, serial ports and high-definition video input.

While less costly, the device also boosts performance over the current BSP-15. Shifting to a 130-nanometer TSMC process, the BSP-16 now runs at 500 MHz, up from 400 MHz, executing up to 8 billion multiply-accumulate functions/second. The chip also consumes an average 1.7 watts, down from 3 W, and measures 60 mm², down from 88 mm². It is the first Equator chip to support DDR SDRAM memory.

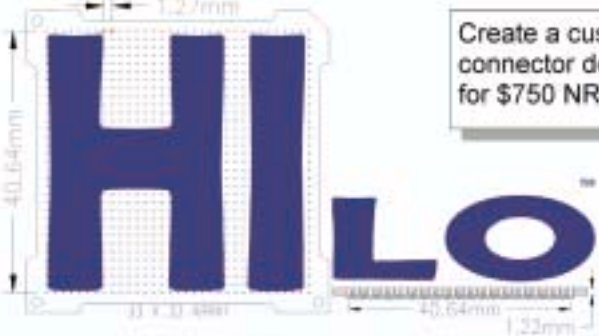
The BSP-16 integrates a 3DES block to support security, especially for a range of supported digital rights man-

agement programs. This includes the DRM that comes with Microsoft’s Windows Media 9. The chip supports AES in software, requiring about 1 percent of the processor’s muscle. Equator is evaluating whether it needs to support AES in hardware in its next generation.

The new chip supports the H.264 video compression codec for standard-definition (SD) video including support for personal video recorder features in SD. High-def video is supported through Microsoft’s Windows Media 9 and MPEG-2 codecs.

The company’s next-generation chip, the BSP-17, expected in the fall of 2006, will support H.264 for high-def. A follow-on part, the BSP-18, will support multiple SD and HD streams for use in a high-def personal video recorder.

Binary-compatible with today’s BSP-15, the BSP-16 is optimized for four-layer pc boards. Hardware reference designs and software tools are available.



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Building Blocks

Low-k strategies

FROM PAGE 36

restrictive design rules, she said.

Even ordinarily aggressive equipment and materials provider Applied Materials Inc. is coming up conservative. Applied senior vice president Farhad Moghadam said that the company exploited the work it had already put into its widely used Black Diamond carbon-doped oxide (SiOC) material. Applied will push k down in increments by gradually increasing the SiOC porosity. This, combined with a redesign of barrier- and seed-layer engineering, will reduce the RC product about 10 percent for each successive node down to 35 nm.

One force behind the growing conservatism is that ultralow-k (ULK) materials are simply not considered ready for prime time, for two reasons.

First is mechanical strength. Generally, the more porous you make a film, the more easily it will bend or fracture under mechanical stress. The first impact of this problem is on chemical-mechanical polishing. Applied has dealt with that by reducing the force on the polishing pad to about 1 gram and using electric current to replace downward force in removing material.

The more intractable mechanical problem is in scribing and packaging, where temperature cycles and mechanical forces attack the surface of the die, often damaging dielectric stacks. "There is a strong interaction between the interconnect stack and the packaging and assembly operations now," Chia-Hong Jan, senior BEOL program manager at Intel, said during an IITC panel discussion. "We need both stronger interlayer dielectrics and lower-stress packaging."

The second issue is time-dependent dielectric breakdown. Because the new materials are porous, if other chemicals from process steps or nearby layers get onto the surface of the low-k materials, they can penetrate them, increasing the k of the material or leading to electrical breakdown. This has mandated agonizing work on arranging the process steps so that the dielectric material is always shielded from other chemicals; engineering barrier layers to isolate the materials from copper; and keeping the whole structure from cracking or leaking.

Process engineers thus have shifted

their attention away from the needs of circuit designers and toward the realities of making reliable chips. "Manufacturability and reliability dominate our decisions," said panelist Robert Wisnieff, senior integration manager at IBM Microelectronics. "We are deciding now in favor of the fewest possible changes, not the most aggressive paths. . . . We are relying on hierarchical scaling—moving rapidly to larger geometries at successively higher metal layers. This

requires help from routing engineers and chip architects."

One ray of hope at IITC came from Fujitsu. An early paper reported fabrication of a complex interconnect stack that used porous ULK materials

on the first seven metal/via layers, followed by four layers of SiOC-based metal at considerably relaxed dimensions and capped off with two even sparser layers using ordinary oxide as the dielectric. Fujitsu described a fabrication scheme that it said afforded both excellent protection against contamination of the sensitive ULK material and—with the right design rules—adequate mechanical strength.

The papers reflected 'a slowdown' in the ITRS.

On-chip dc/dc

FROM PAGE 34

But voltage supplies are not within the normal range of IP. They are mixed-signal designs, often done in large-geometry processes with access to good analog transistors and safely kept on their own substrate to avoid noise or thermal coupling to the circuits they serve. And, especially in battery-supplied applications, they need to be as efficient as possible while tolerating a wide input voltage range. Not the kind of new block one undertakes to integrate lightly.

LTRIM is trying to change that perception. Last week, the company introduced a line of dc/dc converter IP blocks intended to be implemented in standard 3.3- or 1.8-volt logic processes in 0.25-, 0.18- or 0.13-micron logic processes. The designs use external passive components and only logic transistors, so they require no special process modules for the SoC.

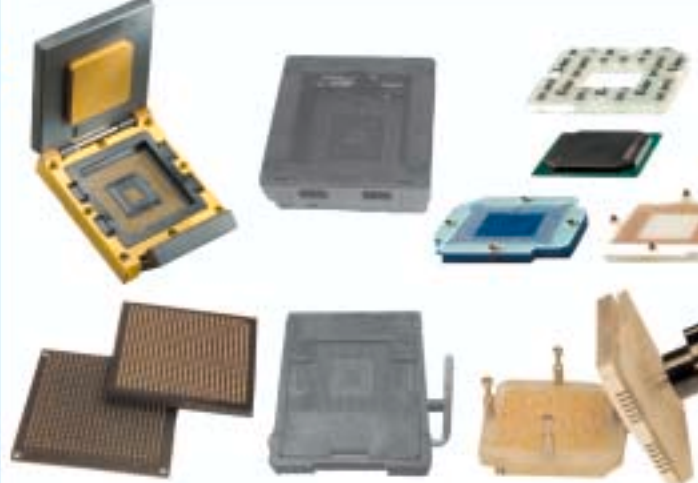
Shamshirian said that there is almost no die area penalty for integrating such modules. "We are talking about maybe 0.4 mm² in additional die area," he said.

Designs will first be available for TSMC's 0.18-micron processes, with 130-nanometer and quarter-micron versions to follow.

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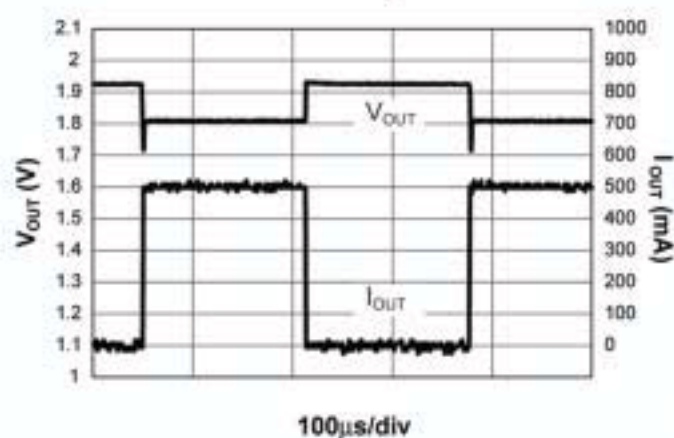
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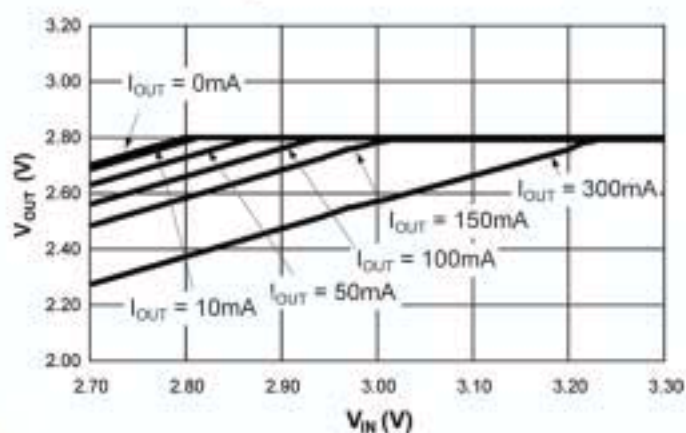
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Accuracy	Dropout (mV) Typical	I_{GND} (μ A) Typical	I_{OUT} (mA) max	V_{in} max	V_{out}	Package
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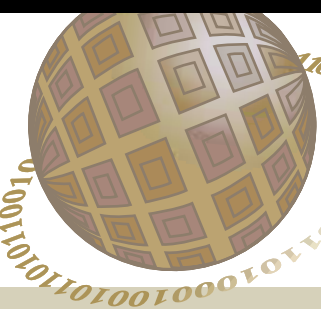
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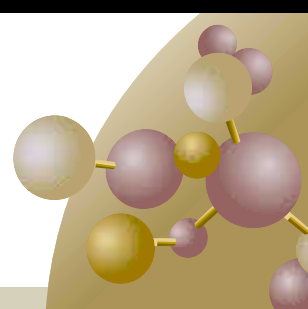
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MIT soft-lithography method harnesses DNA

Project borrows 'nature's printing technique' to transfer pattern to substrate

By R. Colin Johnson

Portland, Ore. — A soft-lithography technique that harnesses deoxyribonucleic acid (DNA) as a self-reproducing template is being developed at the Massachusetts Institute of Technology's Supramolecular Nano Materials Group. Researchers in the SuNMag project have demonstrated a self-assembling method, dubbed nanocontact printing, that transfers subnanoscale patterns from a master wafer to any number of production wafers. In doing so, the method sidesteps the problems of both photolithography and nanoimprinting.

"What we have developed is a method that is able to reproduce DNA patterns from one surface to another," said materials scientist Francesco Stellacci, who heads the project. Stellacci, who describes the technique as using "DNA strands as Gutenberg movable type," performed the work with EE professor Henry Smith, EE graduate student Tim Savas

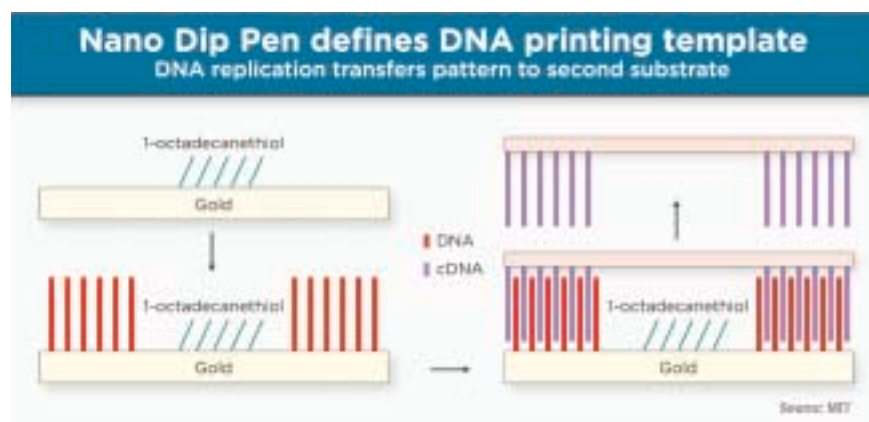
nar surfaces and offers no controls over the chemistry of materials.

Whitesides' brand of soft lithography attempts to solve those problems by creating molecular-scale patterns through molecular self-assembly in SAM films. In a nutshell, Stellacci is using DNA as a submicrometer duplication process that offers a means of transferring design features that are beyond the reach of other soft-lithography approaches.

"Nature takes DNA double helices, separates them into single-stranded DNA, then copies the whole genetic information onto a strand of RNA," said Stellacci. "This is a printing method, if you think about it, that is comparable to photolithography because it takes information from one point to another one, like lithography. But it is much better because it has subnanometer resolution, works at room temperature, does not require special chemicals and transfers a lot more information."

Once the DNA is patterned across a wafer, for instance, there are many methods already available with which to convert the organic material into semiconductors, metals and insulators.

According to Stellacci, it should be pos-



able genetic-engineering tools to build a particular DNA sequence that will later be used to, say, fabricate a subnanometer transistor channel. First the DNA is patterned on a substrate using SAM techniques. Next, each strand produces a complement strand to which it is attached. The far end of the complement strand is modified chemically so that it will adhere to a substrate.

"We actually start from single strands of DNA; then we hybridize a complement of that DNA. This complement has a sticky end on the top part, so when we place a surface on top of our pattern, our surface binds to the sticky end of the DNA.

"We then do the same thing that nature does: We tell the DNA to dehybridize, and the two DNA strands separate, giving us a copy of the original pattern on the second substrate," said Stellacci.

Because the original substrate is unmodified by the process, it can be repeated, printing press-style, to churn out endless copies. To control the creation of DNA patterns, the researchers have been using nano Dip-Pen lithography. Developed by Chad Mirkin at Northwestern University, the technique can paint virtually any chemical compounds onto substrates with nanometer control. The demo process used X-ray lithography to define a grating used to transfer an array of DNA wires.

Resolution challenge

Even though the DNA itself measures in angstroms (one-tenth of a nanometer), today Stellacci's prototypes can only achieve about 40-nm resolution. He has high hopes of improving this resolution in future prototypes but says the fairly clumsy genetic-engineering tools currently available may never match the angstrom resolution commonplace in the natural world.

"Today we have a resolution of 40 nm, which is much better than any other soft-lithography method," said Stellacci. "But we may never be able to match nature."

Even at 40-nm resolution, Stellacci's

method offers the advantage of self-assembly. By contrast, other soft-lithography techniques must repeatedly stamp an imprint across a wafer to pattern such elements as transistor channels, gates and interconnection lines.

Eventually, using Stellacci's method, complete three-dimensional cells could be patterned in a single step, instead of requiring the repeated application of different masks (as in photolithography) or the repeated application of stamps (as in nanoimprinting).

"The real beauty of our approach is that the DNA finds its own complement on the surface, so that you can copy as many sequences at the same time as you want. At the end of the day, you end up with a pattern composed of many different sequences, but it only takes one step to print them all at once," said Stellacci.

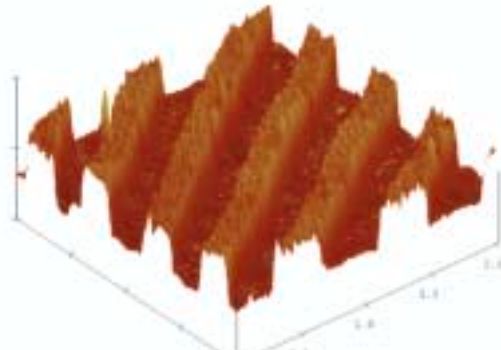
Subnano fabrication

The technique is still immature, said Stellacci, but he predicts that it could become commonplace for the subnanoscale microchips that will be fabricated about 10 to 15 years in the future.

Stellacci talked about the substrates he plans to use next. "Right now, we are printing on a gold substrate—a conductor—which is not good for electronics. But already in the pipeline we have a method for printing on insulating substrates like glass or silicon dioxide, as well as on polymers," said Stellacci. "Then we want to self-assemble complete single-electron transistors."

The project is being funded by MIT's Deshpande Center, which supports the development and commercialization of biotechnology, information technology and nanotechnology. Now that the process has been demonstrated to work, the center plans to spin out a company based on the technique targeted at the gene-chip array market.

The nanocontact printing process is expected to be 10 times more cost-effective than current processes, the center claims in a statement on its Web site (see <http://web.mit.edu/deshpandecenter>).



Atomic-force microscopy image (left) and 3-D rendering of DNA wires stamped on a gold substrate in process pioneered by Francesco Stellacci.

and materials science graduate student Amy Yu. Yu described Stellacci's new method as marshaling "nature's most efficient printing technique: the DNA/RNA [ribonucleic acid] information transfer."

The method is based on previous research into self-assembled monolayers (SAMs) that was conducted by George Whitesides at Harvard University. More than a decade ago, Whitesides began developing an alternative to traditional photolithography. His "soft lithography" circumvents the traditional problems encountered with submicron resolution of design features on advanced microchips.

Photolithography is limited by the optical diffraction and high intensity of the extreme-ultraviolet wavelengths necessary to image nanoscale design features. In addition, photolithography can only be applied to two-dimensional pla-

sible someday to pattern entire wafers with subnanometer designs in three dimensions using his method.

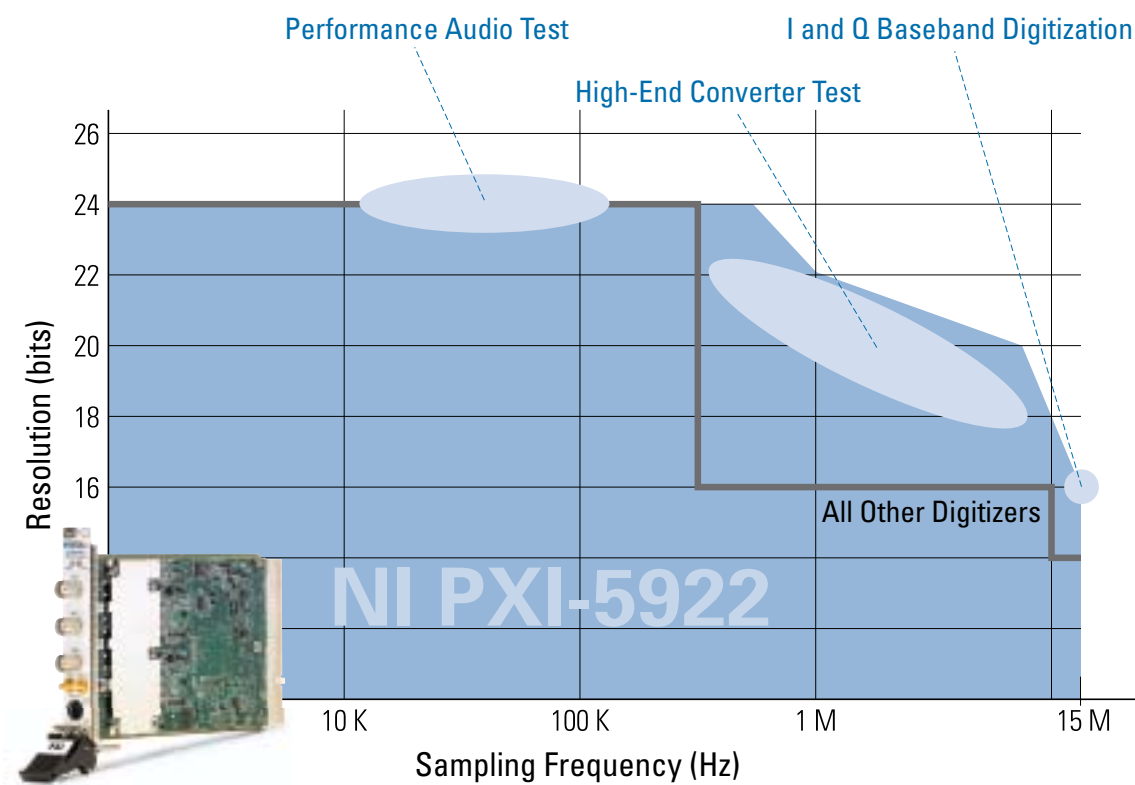
"There is a huge amount of literature out there that already shows you how to convert DNA into useful devices," Stellacci said. "So once you print the DNA, you don't have to use it as such, because there are known methods to convert it, for instance, into silver wires or to assemble semiconducting nanoparticles on top of DNA for single-electron transistors.

"And because you can print many different sequences simultaneously, you could imagine converting some sequences into a wire, and another sequence could assemble a nanoparticle," Stellacci added. "In the end, you get subnanometer-resolution transistors entirely from self-assembly methods."

Stellacci's method uses widely avail-

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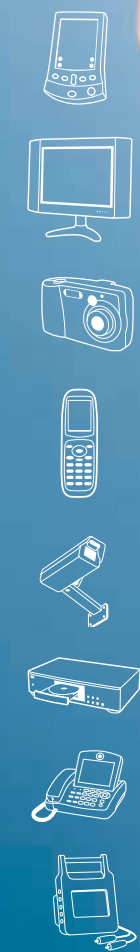
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Dell pushes thin and light for notebooks

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Select the right FPGAs for signal integrity

Embedded Insights: ESL adoption slow

The search for semiconductor IP INTENSIFIES

BY RON WILSON

Simple arithmetic can show the necessity for intellectual-property reuse in system-level chip design. A modest system-on-chip requires millions of gates. Each designer is capable of averaging perhaps a few tens of fully verified gates per day. Unless substantial portions of the chip are reused from previous designs or licensed from third parties, either the design team will grow to the Intel-esque scale or the schedule will span a geological time frame.

But arithmetic doesn't capture the enormity of finding, qualifying and reusing IP. In reality, by many accounts, the industry's

experience was initially horrendous and has since improved to the merely dreadful.

"The situation is so bad that we consider all IP defective by definition," Naveed Sherwani, president and CEO of ASIC venture Open Silicon, stated during a panel at the recent International Symposium on Quality Electronic Design. "We have an internal IP quality group that not only investigates the IP and the vendor, but surveys previous users to try to anticipate the problems."

Nor is Sherwani unusually pessimistic. Colin Harris, vice president of worldwide operations at PMC-Sierra Inc., said his

CONTINUED ON PAGE 51

Even when a viable candidate is found, verifying the intellectual property can freeze a design cycle



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Design Currents

TechTrends

Evaluating IP

FROM PAGE 49

organization has made a policy of acquiring IP for supposedly stable blocks, such as standard interfaces, where PMC's engineers could add little customer-visible value and where one would think IP quality should be reasonable. But "we typically spend about a third as much on IP evaluation as we do on the purchase itself," Harris said.

"Clearly, buying IP today is still risky, despite all the internal approaches to evaluation that large companies have put in place," lamented Ralph von Vignau, director of technology and standards at Philips Semiconductors.

Courtship 2005

For vendors and users alike, the IP selection process has become much like courtship by Internet: You don't really know who's out there. And if you change your mind once you've made your choice, the cost of breaking off the relationship makes even the lousiest divorce settlement pale by comparison.

One of the most formidable undertakings for any SoC design team today is the identification, evaluation and selection of IP. If the choice is poor, at best the team may overlook a product that would have saved it much time and effort. At worst, a single IP choice destroys the project.

Today nearly every large-scale user of IP has its own approach for dealing with this risk. The process often involves market searches, checklists, interviews and internal evaluations. It may extend to audits of the vendor's claims, mandatory test silicon and virtual attachment of ven-

functional specifications and the design's functional requirements. Another, equally important, is that the IP can be implemented in the current design since it is compatible with the user's flow and the intended process.

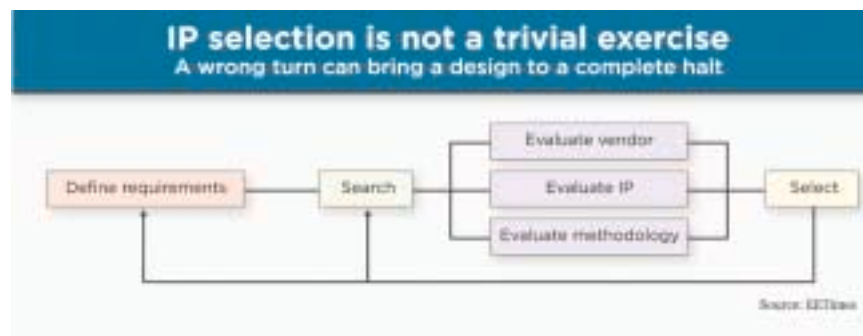
But there are less technical aspects of this evaluation as well. Can the vendor provide enough support to the design team during the IP integration process? What about during ramp-up, when process understanding is vital? Does the vendor have a viable business, or will the IP be orphaned sometime during the project?

The problem in finding an IP vendor for most functions is a superabundance of

one-off research project for each new piece of IP being considered. Many offerings can be disposed of quickly, narrowing the search to IP that could be appropriate to the project.

From the vendor's standpoint, the benefit is at least equally strong: Answer a single set of questions once, and you have on hand the data necessary to begin the discussion with almost any potential licensee. "This can really minimize the work for smaller suppliers," said Saverio Fazzani, technology director at Cadence Design Systems Inc.

Victor Berman, Cadence group director for language standards, added, "It's



riches. Several major companies have made it their business to gather up huge libraries of IP, any of which can contain almost any industry-standard function. But especially in emerging areas or for unusual functions, small players may have important offerings. The problem for vendors and users alike is just getting noticed.

Search and screen

One help in this area are IP exchanges, such as www.us.design-reuse.com, partially owned by CMP Media LLC, the publisher of *EE Times*. Such sites make it possible to search IP listings by function. But finding a nominal match in functionality is far from the end of the job. Identifying vendors of, say, USB 2.0 IP blocks is only the first snowflake in an avalanche of questions to ask.

"There are way too many small providers of IP," said Michael Kaskowitz, president of the Virtual Socket Interface Alliance (VSIA) and general manager of the Inventra division at Mentor Graphics Corp. "You need some kind of metric to help sort through the offerings."

Thus, most IP users write a checklist—or several of them—to help do a quick estimation of IP suitability. The problem with that solution from the vendor's perspective, particularly for small vendors, is that each prospective customer has its own checklist. All the checklists may be superficially similar, but each requires a separate effort on the vendor's part during an evaluation. That has led to calls for a uniform IP evaluation checklist.

Early this month, the VSIA announced just such a list, QIP Metric version 2.0. The concept presents a standard set of questions that can lead a user through a thorough first-pass inspection of any piece of IP. From the user's point of view, the initial phase becomes a routine, instead of a

more than just convenience. Without a standardized process such as this, the finite resources design teams have to devote to the IP search would mean that some vendors would not get a positive hearing. And a situation in which only the large vendors get heard stifles innovation. It defeats the whole purpose of a third-party IP market."

One noteworthy feature of the QIP approach is its scoreboarding capability. The user can assign weights to the answers to each question in the spreadsheet and, after answering the questions, get a cumulative score for a particular vendor and IP offering.

Small differences in scores can be the beginning of valuable conversations between user and vendor. "A big advantage to the QIP Metric is the communications it creates," said Kathy Werner, reuse manager at Freescale Semiconductor Inc. "Two vendors may end up with similar overall scores on the metric but with strengths and weaknesses in different areas. With the metric, you have a quantitative way of discussing what the vendor needs to do to better meet your needs."

A manager at one IP vendor commented that the QIP Metric can also serve as a diagnostic for one's own marketing process. Walking through the QIP process, the vendor gave itself a very good score on a particular piece of IP, while the prospective user gave it a mediocre score. "It showed us very clearly that we had failed to communicate a lot of what we knew about the IP to our prospect," the manager said.

Gross differences in score can be a basis for eliminating a piece of IP—or a vendor—from consideration. So there is a motivation for vendors to tweak either their processes or at least their answers

CONTINUED ON PAGE 64



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Design Currents

TechTrends

Making the best use of formal analysis

Using the right methodology for applying and employing products within a design project is critical to getting a high return on investment. This is especially true in emerging areas such as formal analysis.

Formal analysis holds the promise of reducing testbench development and simulation cycles while improving design verification. Formal analysis uses sophisticated algorithms to conclusively prove or disprove that a design behaves as desired for all possible operating states. Desired behavior is not expressed in a traditional testbench, but rather as a set of assertions. Formal analysis does not re-

By Paul Hylander (hylander@cadence.com), architect, **Axel Scherer** (ascherer@cadence.com), senior member of consulting staff, and **Ramesh Mayiladuthurai** (rameshm@cadence.com), technical marketing manager at Cadence Design Systems Inc. (San Jose, Calif.)

quire user-developed test vectors, but, instead, analyzes all legal input sequences concurrently and automatically.

When applied correctly, formal analysis improves productivity and reduces time-to-market. With formal analysis, many bugs can be found quickly and very early in the design process without the need to develop large sets of test vectors or random test generators.

Furthermore, because of its exhaustive nature, formal analysis improves quality by finding corner-case bugs often missed by traditional testbench-driven verification. The dual benefits of increased productivity and increased quality are driving the adoption of formal analysis into the design flows of many companies.

The adoption of formal analysis is a relatively recent phenomenon, enabled by the confluence of several factors. These include improvements in usability, the recent availability of industry-standard assertion languages, and

advancements in performance and capacity. While these factors have enabled formal analysis to transition from the academic into the commercial realm, full mainstream adoption has been limited

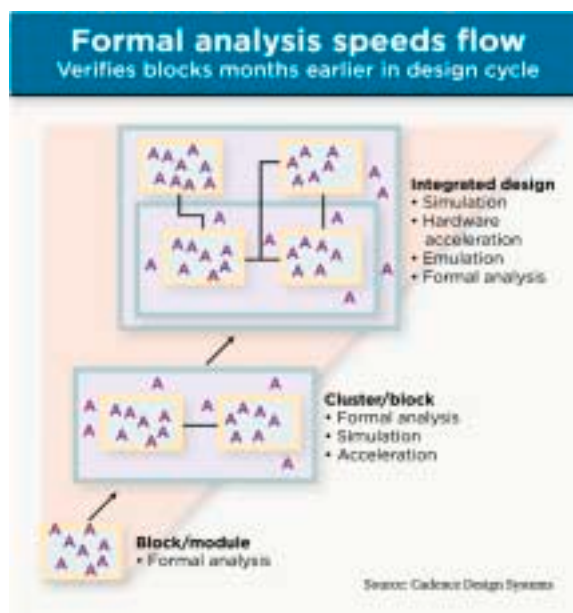
primarily because of the lack of an adequate methodology.

Methodology overview

There are distinct levels of methodology. At the highest level, project methodology integrates formal analysis with the project flow. It involves a description of who on the team performs what activities, when those activities are scheduled and how they will be done. Lower-level methodologies include property coding and RTL design guidelines for formal analysis.

A successful formal analysis methodology has several key elements. The first is that formal analysis must be used in the context of a comprehensive assertion-based verification flow—which includes formal analysis and simulation—and can be extended to acceleration and emulation. These different verification techniques complement one another when used together in a flow.

The second element is that formal analysis should be used on parts of the



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design where the methodology's key advantages can be leveraged efficiently.

The final element is the most crucial one—the people. Design and verification engineers must be trained in the use of the flow and execute it in activities specific to their respective roles.

Verification flow

Three important factors influence the deployment of formal analysis as part of a comprehensive verification flow.

The first and most important factor is that formal analysis does not require test vectors. This implies that engineers are able to start the verification process during the design stage, without investing effort in creating test vectors or writing random testbenches. With this reduced effort, there is little reason not to perform module and block-level verification with the help of formal analysis.

Second, it is important to note that with industry-standard assertion languages (and the corresponding software that supports them), assertions written at one level of a design can be used in many other levels throughout the verification flow. This allows any investment in writing block-level assertion and formal analysis to be leveraged by the other ver-

ification products deployed later in the verification flow.

Finally, formal analysis is exhaustive. On one hand, this aspect of formal analysis makes it very efficient in finding subtle, corner-case bugs in a design. On the other hand, the countless state permutations explored by formal analysis technology hit computational limitations, making it important to choose verification targets carefully to maintain a good return on investment (ROI).

The recommended methodology—assertion-based verification—takes into account the three important factors mentioned above. In this methodology, designers write assertions as they develop the RTL. Then the designers verify these assertions, along with automatically extracted assertions, using formal analysis on their own blocks. This occurs before simulation and before the blocks are integrated into higher levels.

In this block-level verification paradigm, formal analysis can add value by verifying the blocks months earlier in the design cycle—as soon as some partial RTL description is available. This ensures that bugs are found early, when the cost of fixing a bug is low. In contrast, with a simulation-only methodology, bugs are often

found late, when the cost to identify, isolate and fix the design is much higher. Moreover, even with very high coverage, simulation may miss subtle, corner-case bugs, leaving them undiscovered until after first silicon.

Because bugs are found so quickly—often in seconds—with formal analysis, the traditional way of fixing a bug and

It finds subtle, corner-case bugs in a design.

rerunning regressions to find more bugs is vastly inefficient. Instead, the designer can use formal analysis to fix a bug and then immediately check to see whether the fix is correct, potentially exposing more bugs. In that way, a block can quickly converge, with high quality achieved in hours instead of days.

At the cluster/block level, formal analysis is still useful, though run-times may increase. At this level of integration,

formal analysis is used alongside simulation and, in some cases, acceleration. Here, simulation helps not only to verify the correctness of assertions but also to check the assumptions that were used during formal analysis of the sub-blocks.

Finally, at the integrated design level, all forms of assertion-based verification products are applicable, depending on the size of the design and the amount of verification necessary. At this level, simulation, acceleration and emulation are the tools of choice, with formal analysis used to expose a few more corner-case bugs.

This is typically done by using formal analysis in addition to simulation and searching for nearby bugs. Although formal analysis can expose some problems this way, at higher levels of integration the effectiveness of formal analysis varies. Therefore, the use of formal analysis at those levels plays a secondary role.

The addition of formal analysis to the verification flow raises the question of whether simulation can be eliminated. When formal analysis is added to the flow, some simulation activities, such as verification of a few special blocks, may no longer be necessary. Most simulation activities will remain, however, particu-

CONTINUED ON PAGE 62

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— Alan Cocconi, AC Propulsion



On April 22, 2005, Earth Day, AC Propulsion’s SoLong Solar Electric-Powered Unmanned Aerial Vehicle (UAV), controlled by twelve PIC18 microcontrollers, flew for 24 hours without making any noise, without consuming any fossil fuels, with zero emissions, and no contribution to global warming. The above photo shows the virtual cockpit snapshot of Alan’s record-setting SoLong UAV.

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						UART	LIN	I ² C™/SPI™	
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PIC18F87J10	32K-128K	10	40	64/80	High-Performance, Low Voltage	2	ã	2	ã
PIC18F4620	4K-64K	12	40	28/40	General Purpose	1	ã	1	ã
PIC18F4550	24K-32K	4	48	28/40	Full-Speed USB 2.0	1	ã	1	ã
PIC18F4680	16K-64K	12	40	28/40/64/80	CAN 2.0b	1	ã	1	ã
PIC18F8490	8K-16K	4	40	64/80	Up to 192 LCD Segment Driver	2	ã	1	ã
PIC18F4431	8K-16K	4	40	28/40	High-Speed ADC Motor Control PWM	1	ã	1	ã

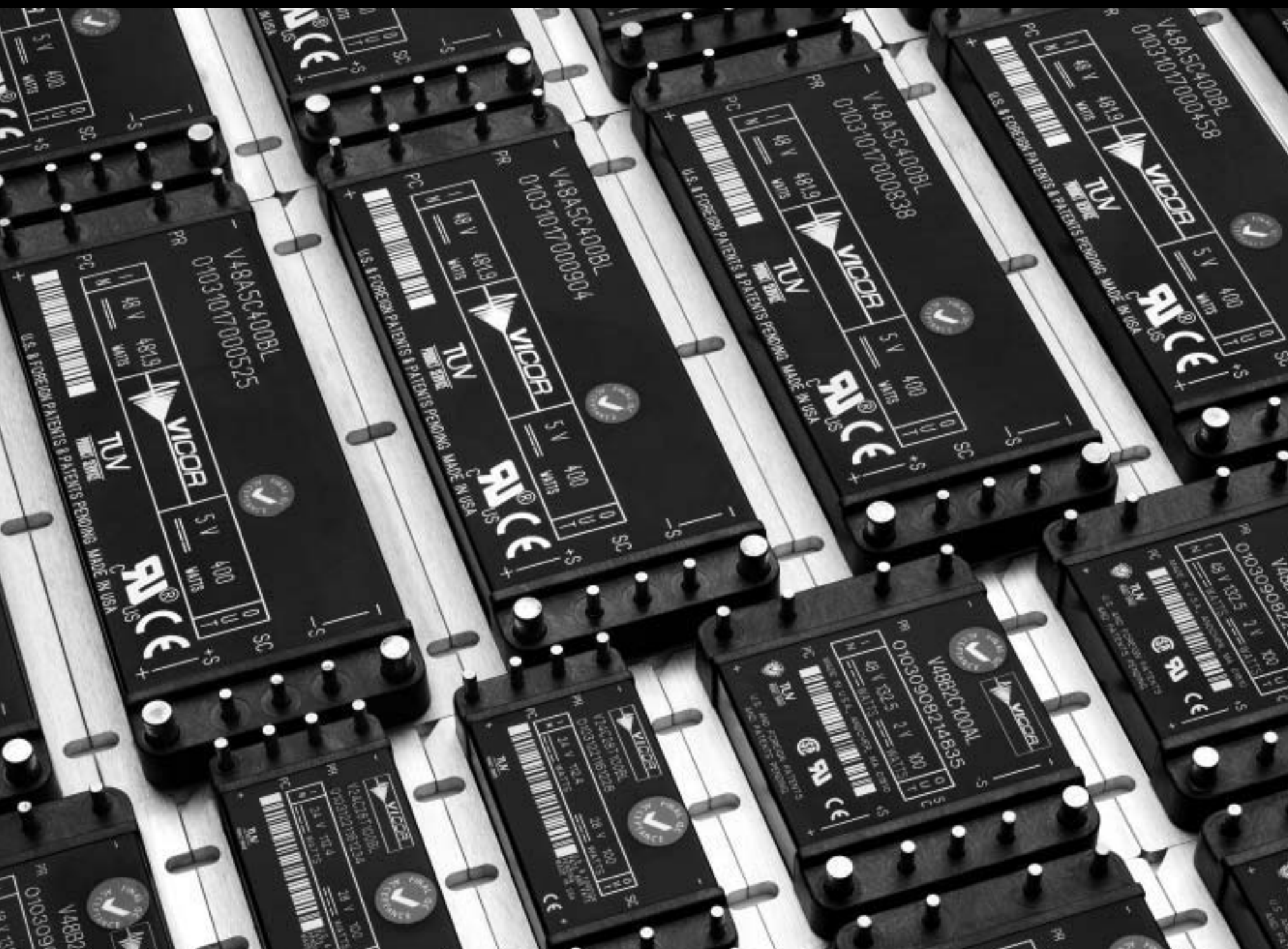


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Design Currents

TearDown

Thin-and-light Dell for the road

With well over 30 manufacturers offering more than a thousand notebook PC models in the U.S. market alone, one niche segment that targets the road warrior is emerging: the sub-14-inch, “thin-and-light” form factor, intended to seduce mobile users everywhere.

In April, sales of thin-and-light notebooks hit new highs, with the systems capturing 30 percent of the retail notebook market. That number reflects the growing popularity of this mobile form factor and the subsequent price drops it has experienced. With more and more people using mobile technologies for work and personal use, manufacturers have been pressed to adopt cost-saving technologies, labor and parts.

To provide insights into the costs of manufacturing and labor for these increasingly in-demand lightweight machines, Current Analysis Labs studied the Dell Inspiron 600m notebook.

Product analysis

The Inspiron 600m houses a 1.3-GHz Intel Celeron M processor, a 60-Gbyte hard drive, a CD-R/DVD-ROM optical drive, 256 Mbytes of DDR SDRAM, and an ATI Radeon 9000 graphics chip with 32 Mbytes of dedicated DDR SDRAM.

The Dell system combines the portability of a thin-and-light laptop with the value of a mainstream consumer notebook. The thin-and-light classification denotes that the machine travels well,

weighing in at less than 6 pounds, but that it still provides utility, with a screen that's large enough to be viewed easily (around 14 inches) and a keyboard large enough to accommodate comfortable typing. In its basic configuration, the 600m weighs less than 5.3 pounds and is only 1.2 inches thick when closed.

Various software packages come pre-installed: Windows XP Home, WordPerfect Productivity, Windows Media Player, H&R Block Tax, Adobe Acrobat Reader, CyberLink PowerDVD, McAfee VirusScan, Music Match, Netzero ISP, Paint Shop Photo Album, Dell Media Experience and a DVD decoder.

Complementing the portability is the Inspiron 600m's standard set of connectivity options to keep the consumer covered in both wired and wireless scenarios. It also includes an integrated modem and network interface. There is no FireWire port, but there are two USB 2.0 slots at the rear of the system for connecting peripherals. There are also the usual monitor-out, serial and parallel ports.

Dell has included a single PC Card Type II slot on the left side of the note-

book, while the right is home to a CD-RW/DVD combo drive.

The Dell Inspiron 600m measures 12.4 x 1.2 x 10 inches and weighs 5.3 pounds. The package contains the notebook, power adapter, power cord, phone cord, catalog, instruction sheet, product information guide and software CDs.

Production cost analysis

Most of us are aware of the lower manufacturing costs that result when IT and consumer electronics products are outsourced, but how much should it cost manufacturers to stay competitive in today's notebook market?

To answer this question, we examined the Dell Inspiron notebook at a production volume of 1.5 million units and assumed the model was produced in Malaysia. To do this, our Labs used time- and industry-tested methodologies to estimate the purchase costs of commodity components, manufacturing costs of fabricated components and location labor rates.

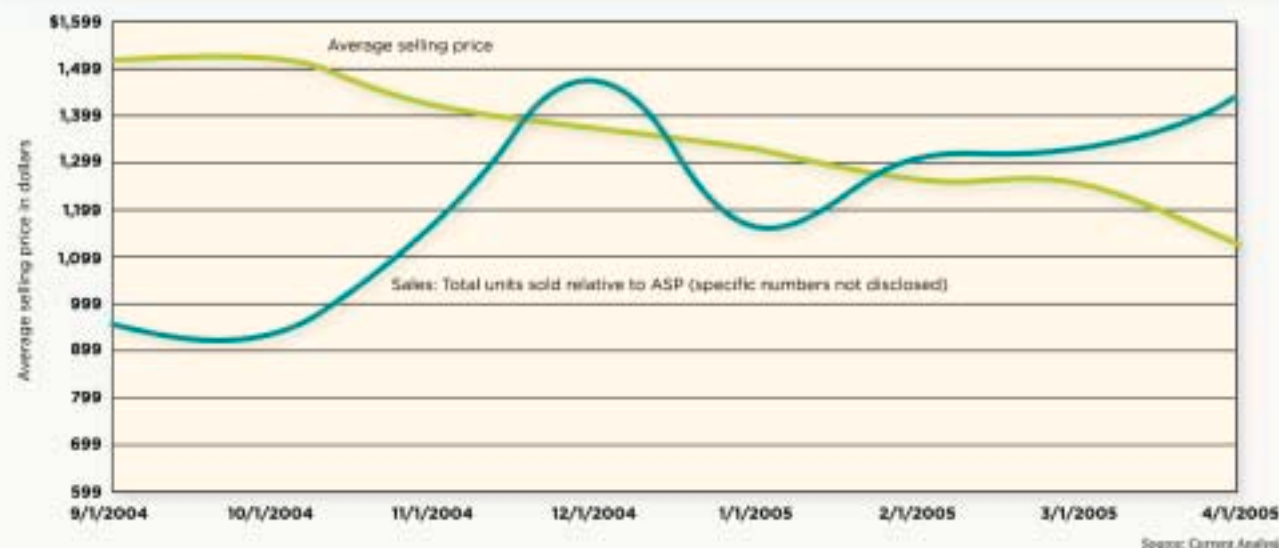
When paired with the least expensive components, Malaysia proved to be an attractive country for manufacturing. Indeed, the final cost per unit was only \$471.85.

Total manufacturing costs broke down as follows:

- packing total, \$14.76;
- electronics total, \$306.97;
- mechanical assembly, \$133.74
- keyboard and accessories, \$15.72
- final prep, \$0.66;
- keyboard and accessories, \$15.72

At present, the manufacturer's suggested price is listed at \$1,217. Under the previously stated manufacturing assumptions, this price delivers a profit of \$745.15 before taxes and other tariffs.

Thin-and-light notebook retail figures
By April, thin-and-lights held a 30 percent share of the retail market



Source: Current Analysis

Market analysis

It is no secret that although the U.S. notebook market has experienced significant growth over the past year, it has also been plagued with price erosion that has drastically narrowed manufacturers' profit margins. During the same time period in which the retail market saw sales growth of 43 percent, the average street price of notebooks decreased by 12 percent, from approximately \$1,399 to \$1,229.

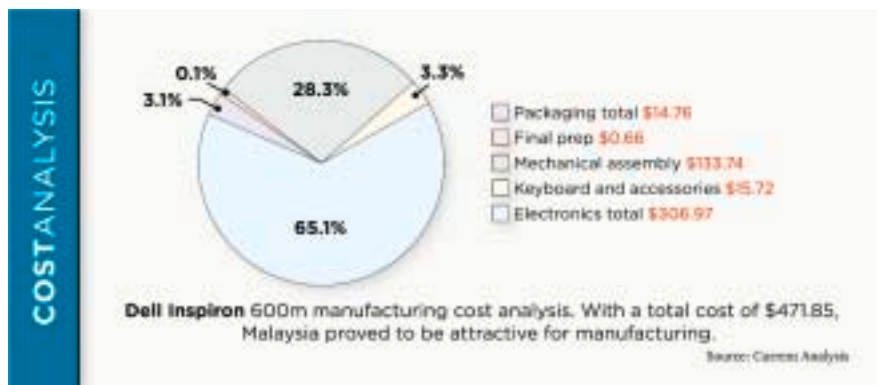
This scenario holds especially true in the rapidly growing thin-and-light segment, particularly since the introduction last October of Hewlett-Packard's Jakarta 14W systems (the dv1000 line). Before October, thin-and-light systems accounted for only 10 percent of retail sales. But by April, thin-and-lights held a 30 percent share of the retail market. That means unit sales of this segment grew by 147 percent between October and April.

Unfortunately for manufacturers' bottom lines, however, the segment's ASP declined by 26 percent, from \$1,517 to \$1,129, during the same period.

The threat of price erosion increases the need for manufacturers to minimize their production costs. With an MSRP of \$1,217, Dell's thin-and-light Inspiron 600m generated an estimated profit of \$745. But to remain competitive, Dell offered a \$400 mail-in rebate on the system, dropping the advertised price to \$817—and its estimated profits to \$345.

CONTINUED ON PAGE 64

By Nicole D'Onofrio
(ndonofrio@currentanalysis.com), analyst for mobile computing at Current Analysis Inc. (Sterling, Va.)



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A series of engineering insights
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Boost Precision and Accuracy with Single Chip Capacitance- and Impedance-to-Digital Converters

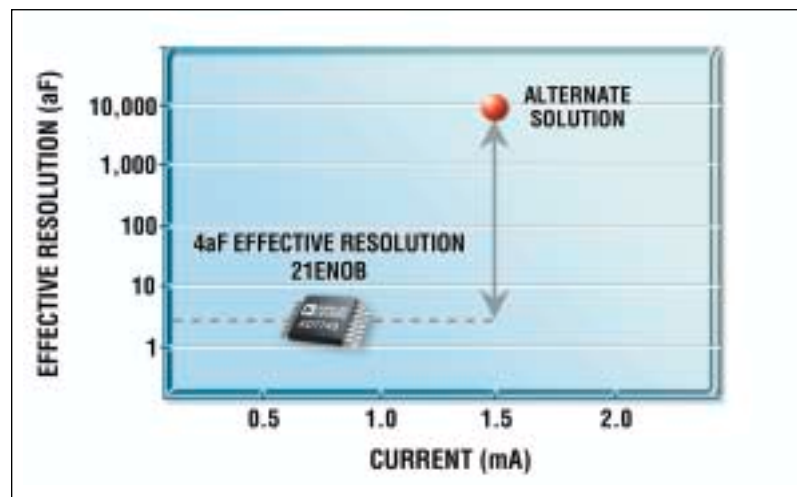
High precision capacitance- and impedance-sensing applications traditionally required a complex collection of discrete components that needed to be skillfully combined together to provide an overall measurement solution. Not only was this time consuming from a component selection perspective but as each application differed slightly, it also required significant design validation, evaluation, optimization, and qualification.

Overcoming Design Barriers with New Converter Architectures

By architecting an optimized solution that incorporates all of the required functionality on a single chip, Analog Devices has created two new converters that provide system level solutions for impedance and capacitance conversion and deliver higher precision and accuracy while reducing size, design time, cost, and power. This advanced level of integration is particularly important when processing small signals where excess noise, component tolerances, and temperature drift can adversely impact measurement accuracy. In addition to providing superior performance, both converters are available in small packages. Applications in the industrial instrumentation, automotive, and biomedical sectors can benefit from higher precision capacitance measurement or simplified impedance analysis—both at lower cost and without the inherent complexities and design limitations of multichip discrete designs.

Convert Capacitive Sensor Signals to Digital with High Precision

The architecture of the AD7745/AD7746/AD7747 capacitance-to-digital converters (CDC), which includes a patented analog front end interface, eliminates the negative effects of external parasitic capacitance. This architecture opens up high performance applications in medical instrumentation (for patient monitoring and blood pressure measurements), in industrial instrumentation (for pressure and level sensors and smart transmitters), and in automotive environments (for position and level sensing, as well as occupancy and proximity detection).

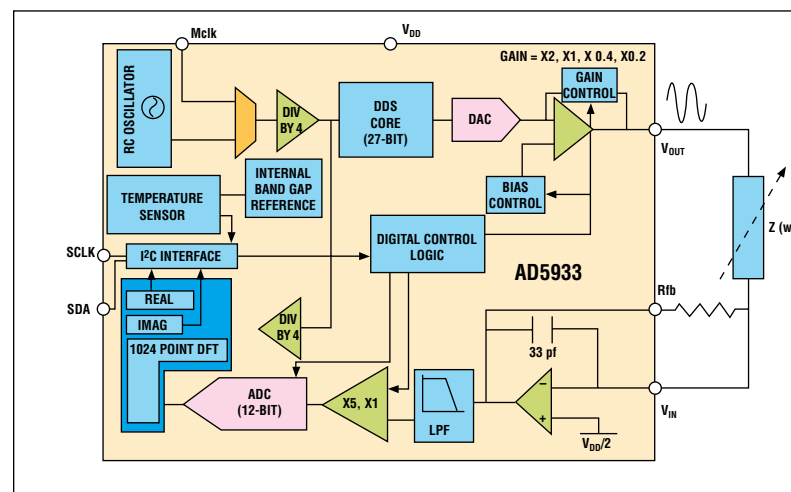


The AD7745 delivers high precision with unequalled accuracy, low noise, and low power.

The CDC is suitable for these applications because of its unique combination of high precision, small package, low power, low cost, low temperature drift, and low noise. The AD7745/AD7746/AD7747 are available in small 16-lead TSSOP packages at 1k unit pricing of \$4.60 (AD7745/AD7747) and \$4.95 (AD7746).

Measure Impedance More Accurately with Mixed-Signal Integration

The new AD5933/AD5934 impedance-to-digital converters (IDC) put direct digital synthesis (DDS), analog-to-digital conversion, and DSP on a single chip. The IDC measures impedances ranging from 100 Ω to 10 M Ω , excited with an on-chip frequency generator of up to 100 kHz. The response signal from the



The AD5933 block diagram illustrates the advanced level of integration contained in its single-chip form factor.

impedance is sampled by the on-chip ADC and its discrete Fourier transform (DFT) is processed by an on-chip DSP. The DFT algorithm returns both a real (R) and imaginary (I) data word at each frequency point (for a sweep), enabling phase and amplitude impedance calculations based on an initial calibration. The AD5933/AD5934 are available in small 16-lead SSOP packages at 1k unit pricing of \$4.35 (AD5934) and \$6.65 (AD5933). For additional product information, go to www.analog.com/CDC and www.analog.com/IDC. ■

Author Profiles: **James Caffrey** is the product marketing manager for the Precision Converter group at Analog Devices, where he is involved with product and business development strategy for low voltage DACs.

Conor Power is the product marketing manager at Analog Devices for the Instrumentation and Automotive Converters group.



Design Currents

Tips&tricks

FPGA choice has bearing on signal integrity

Signal integrity has become a critical issue in the design of high-speed systems. Inferior signal integrity leads to poor reliability, degraded performance, field failures and delayed product releases—all of which can trigger lost opportunities and revenue. It can arise from a variety of issues at the chip, package or board level. Chip-level concerns include improper I/O buffer design and inadequate return-current paths. Package-level issues include high package inductance, mismatched traces, improper routing and inadequate return-current paths, while board-level issues include crosstalk, reflections, signal attenuation and EMI/EMC.

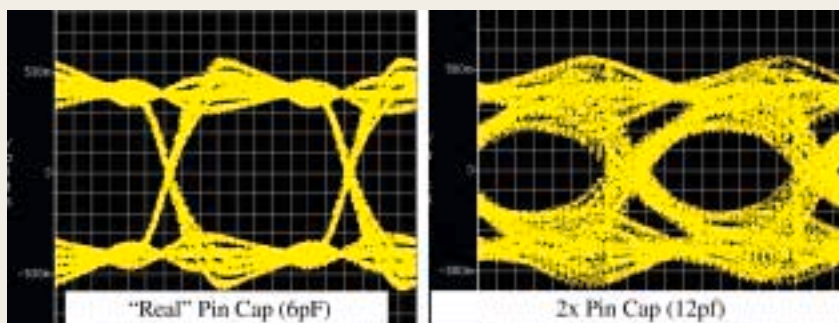
Signal integrity is a key criterion when selecting FPGAs for high-speed applications. To support a range of applications, today's FPGAs support a variety of single-ended and differential I/O standards, with options to control drive strength, slew rate and on-chip termination. The flexibility offered by FPGAs can make it difficult to manage signal integrity compared with ASICs or ASSPs. Some FPGA vendors have made significant efforts to design packages and chips that provide robust signal integrity.

This article will detail the do's and don'ts that system designers should keep in mind when selecting the right FPGA to ensure sound signal integrity within a given design.

By Lalitha Oruganti
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I/O technical
staff at Altera
Corp. (San
Jose, Calif.)



- **Anticipate possible signal integrity challenges early in the design cycle.** With how many devices will the FPGA interface? What are the interfaces' bus widths and performance? What are the critical high-speed signals? Which power supplies are required? How can the system be designed (including pin assignment, board routing, board stackup, termination, power decoupling and impedance matching) for robust signal integrity?
- **Find out the FPGA design methodology.** Was mitigating signal integrity a key criterion during the device planning and design phases? What are the device and package features in the FPGA that will reduce signal integrity failures?
- **Make sure the vendor has correlated I/O buffer and package Spice or Ibis models.** Ask for correlation data that shows that the simulation results with these models match lab experiment data. Such data proves the vendor has done sufficient signal integrity analysis.
- **Ask the vendor for in-house signal integrity characterization results.** Signal integrity tests include signal eye diagrams, I/O toggle rates, I/O edge rates (rise and fall times), jitter, I/O pin capacitance, simultaneous switching noise and link-level performance. Each test offers important signal integrity information. For example, high pin capacitance affects signal integrity because of reflections.
- **Ask the FPGA vendor to provide a demonstration board to perform signal integrity testing.** If test results are satisfactory, try to use the demo board Gerber files as a baseline for your board design. Also ask the vendor for termination recommendations, board guidelines, and I/O placement and chip design recommendations.



Shown is 1.0-Gbit/s LVDS IBIS eye-diagram comparison of FPGAs with "real" pin capacitance and FPGAs with twice that pin capacitance.

Source: Altera Corp.

- **Decide on a vendor without doing a thorough analysis of the FPGA design methodology, design features and device characterization data.** Signal integrity tools and support offered by the FPGA vendor must be evaluated. Tools and support include I/O models, pin placement and board design guidelines, demonstration boards and sample Gerber files.
- **Let the system timing margin cut close to zero.** Make sure that the design has sufficient margin to run reliably at the desired frequency under all operating conditions. When performing timing margin analysis, assume worst-case numbers. Signal characteristics vary under varying temperature and voltage conditions. Having sufficient timing margin will ensure the robustness of the system.
- **Ignore the I/O programmability features that the FPGA offers.** Today's high-density, high-performance FPGAs provide programmable drive strength, slew rate and on-chip termination settings for single-ended and differential I/O standards. Using the right setting for your system helps provide the optimal signal quality and amplitude. The best way to determine the right setting for a specific application is to perform Ibis or Spice simulations.
- **Compare signal integrity results of different FPGAs without understanding the test setup.** To get a proper comparison of signal integrity performance among multiple FPGAs, take into account differences in test conditions, board setup and test pattern. Minor variations in the setup can have a significant impact on signal integrity.
- **Build a board without performing simulations to predict signal integrity in your system with multiple FPGAs.** While performing simulations, take into account board trace impedance, trace length, vias, on-board termination and any other board components that will impact signal integrity. This step prevents expensive and time-consuming board respins.

ImpulseResponse

Making benchmarks truly useful

Last month, I took part in a panel discussion on benchmarking. The theme was how to benchmark multithreaded and multicore processors. In my view, this theme highlights a key problem with many benchmark approaches: Too many benchmarks are designed to exercise hardware features, rather than to provide information that system developers need.

In most embedded applications, system developers care about high-level system attributes, such as low cost, long battery life and high throughput. System developers generally don't care *how* a solution delivers these top-level attributes; they care only about *how well* it does so. Therefore, benchmarks should be built from the top down, based on application requirements—and not from the bottom up, based on preconceived notions of what sorts of hardware will be used in the application.

Steer clear of assumptions

More generally, benchmark designers should avoid making assumptions about the hardware whenever possible. In many embedded applications, such as the signal processing applications on which my company focuses, system designers have great latitude to select among very different kinds of processing engines. A benchmark designed with one of these classes of hardware in mind is unlikely to give valid results for the other classes of hardware. Therefore, a benchmark that makes unnecessary assumptions about the hardware will have limited utility.

In fact, the need for flexibility extends beyond accommodating all of the hardware options. To be truly relevant, a benchmark also must accommodate the full range of implementation techniques used in the application. For example, developers of signal processing applications almost never build an entire application with plain C code. Even the best compilers sometimes produce very inefficient code, and when they do, a

CONTINUED ON PAGE 60

By Jeff Bier, president of Berkeley Design Technology Inc.
(www.BDTI.com), a consulting firm providing analysis and advice on DSP technology. Kenton Williston of BDTI contributed to this column.

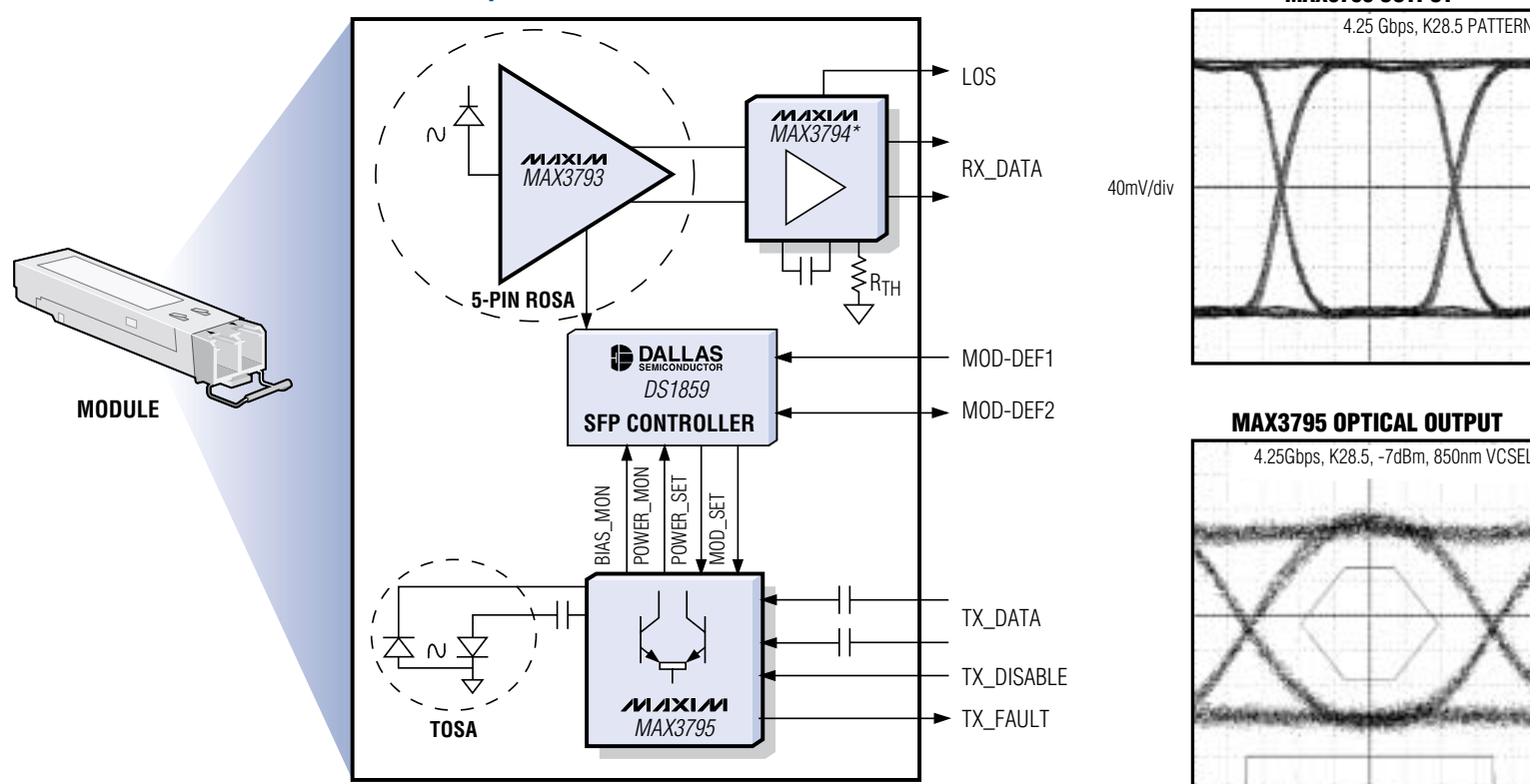


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Design Currents

Tips&tricks

Benchmarks

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skilled programmer often can make vast improvements with modest effort—perhaps by modifying the C code or by replacing portions of it with assembly code. As a result, a benchmarking approach that relies on plain C code is unlikely to produce useful performance data for signal processing applications.

Another problem with using C—or any other programming language, for that matter—is that this approach isn't appropriate for solutions such as FPGAs, which do not run "software" in the traditional sense. Of course, there are many applications where the best approach is to use an FPGA or other solution that doesn't rely on software. Hence, benchmarks should avoid narrowly specifying the imple-

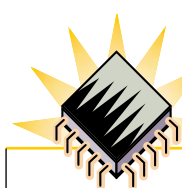
Benchmarks should model the requirements of the application.

mentation methodology to avoid excluding relevant hardware options.

In summary, setting out to create benchmarks for a specific implementation approach—such as using multi-threaded processors or plain C code—is going about things the wrong way.

Instead, benchmarks should model the application requirements and leave the implementation approach (multiprocessing, multi-threading, reconfigurable hardware, hardwired solutions, or what have you) to the benchmark implementer—just as actual applications allow for many different implementation approaches.

Benchmark developers who find themselves designing benchmarks to show off particular features of particular kinds of hardware should ask themselves whether the results are really going to be meaningful. And system designers need to understand the design of a benchmark before accepting and using the results that the benchmark produces. If a benchmark assumes a specific hardware feature or a specific implementation methodology, system designers should proceed with caution.



Embedded insights

Views from the horizon of engineering and design

Innovation and inertia, equally

By Jim Turley

We're creatures of habit, doomed to repeat little routines until the end of our days. Programmers have certain code conventions they follow, hardware engineers adhere to familiar design techniques, and managers, well—they internalize robust new out-of-the-box paradigm methodologies to motivate us.

Nowhere is this rut more evident than in embedded design. Ironically, the very industry that thrives on constant innovation and change is deeply mired in old habits. We talk about innovation but we're stalled by inertia.

Take electronic system-level (ESL) design tools and their slow rate of adoption. On an academic level, ESL sounds great: Design your hardware and your software all at once. Have a single tool crank out the chips and the code. Just about every engineer lubricated by a few beers has waxed enthusiastic on the concept at some time. It's design elegance itself; what's not to like?

Jim Turley
(jturley@cmp.com) is
editor in chief of
Embedded Systems
Programming,
a sister publication
of EE Times.



Except that we don't do it. We go back to our old ways, hammering out code line by line, or drawing schematics, or writing Verilog. We compose, compile and decompose (debug) in an endlessly iterative rotation of anticipation and disappointment. ESL might as well be "English as a second language."

Three's the limit

That's because we're only human. Inertia is in our nature. A sociologist friend says that specialists, no matter what their profession, can change their skill set only three times in their career. Whether you're a doctor, an architect or a programmer, she figures you can only adopt new tools or new skills about three times before you retire. For a doctor, that might mean learning new diagnostic techniques or rethinking how a certain class of diseases is treated. For an architect, that might mean shifting from a drafting board to AutoCAD to something new. For programmers of a certain age (ahem), it usually means upgrading from assembly language to C (or Fortran, Algol, Cobol, Pascal; take your pick) to some new language. And for hardware engineers, it usually encompasses the shift from schematics to hardware-design languages (Verilog or VHDL) to something new. And unless you're in the final third of your career,

you're likely not ready for that final shift.

It's not that we're obstructionist. We just resist change. Professional skills are hard-won and not easily surrendered. One day you're the device driver guru; the next day you're an unproductive beginner learning a new programming language/tool/paradigm. Somewhere there's a really good buggy-whip maker; he just doesn't get a lot of new work.

The same phenomenon also explains why young startup companies often leapfrog older firms. An older corporation (from the Latin for body) is just too old; it's made its life changes already and has a hard time making yet another. Younger companies don't have that institutional memory; they're still spry and limber. But even at the personal level, we have a hard time adopting all the change that we ourselves create.

It's frustrating for the makers of new tools, new programming languages and new types of chips. "Why doesn't the world just get it?" they cry. "Why don't our fellow engineers see the advantages to this new approach?" Because, Gentle Reader, we're still just hairless apes, recently descended from the trees. We don't like to change, much as we may say otherwise. It's a profound paradox in our industry that we promote change much more rapidly than we ourselves can adopt it. Keep up the good work.



Revving video encoding on C64x/DM64x DSPs

How does one improve video encoding performance on the Texas Instruments TMS320C64x/TMS320DM64x digital signal processor generation?

The conventional implementation of a video encoder (MPEG-2, MPEG-4, H.263) is based on macroblock-level processing. The video encoder fetches a new macroblock (MB) only after the current MB goes through all the processing steps. But this intuitive approach comes with two drawbacks:

- The overall code size of a video encoder is usually bigger than the Level 1 program cache (L1P) on a C64x/DM64x DSP. The code needs to be swapped between L1P and the Level 2 program cache (L2P) during every MB fetching period, causing a significant cache-miss penalty.

- It is not efficient for the enhanced DMA (EDMA) controller to transfer a small chunk of data such as a single MB from an external video

frame memory to internal memory.

To avoid the huge cache-miss penalty and CPU stalling, the algorithm can be broken into three loops, each of them a separate module that fits into L1P. Instead of processing a single MB at a time in each loop, the module processes n macroblocks—an MB strip. The size of a strip is restricted only by the size of the available Level 1 data cache (L1D). The bigger n is, the better EDMA performance we can expect for data throughput.

The three loops are:

- the MB encoding loop,
- the motion estimation loop, and
- the MB reconstruction loop.

As emphasized above, n MBs are fetched and go through one of the three processing loops together.

For example, in the MB encoding loop, when n MBs are fetched into internal memory, they are put through a discrete cosine transform

(DCT), quantized and entropy-coded. This set of macroblocks is not flushed out of L1D until the MB encoding loop has been completed. Corresponding programs, including DCT, quantization and variable-length coding kernels, are also kept in L1P until all n MBs are processed completely in this loop.

A ping-pong memory buffering scheme driven by the EDMA helps reduce the initial setup time needed to perform these loops for a strip of MBs. Ping-pong buffering also ensures minimal CPU stalling cycles because the transfers are overlapped with processing.

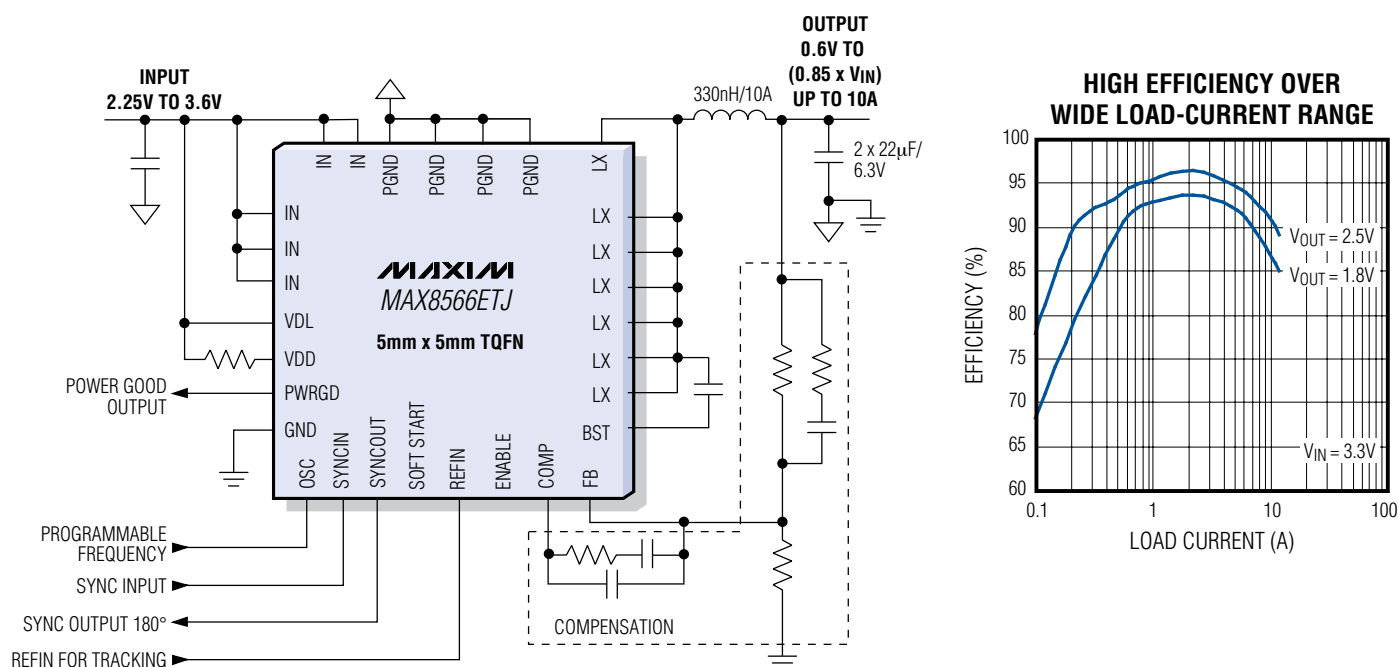
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Design Currents

TechTrends

Formal analysis

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larly for integrated design verification.

Using formal analysis at the block level is a key factor in increasing ROI. Some blocks are better suited for formal analysis than others. The main consideration during block selection is the amount and complexity of control logic in a block.

Control logic blocks tend to have many corner cases and have high potential for subtle bugs, making them great targets for formal analysis. These include, among others:

- Interacting state machines,
- Arbitration,
- Pipelined control,
- Speculative operations and
- Exception handling.

These sorts of blocks are excellent candidates for formal analysis because it's unlikely that even good directed-random testbenches will hit all possible corner cases. Formal analysis, on the other hand, can very efficiently verify such logic.

Designers should also consider the presence of data paths and memories. Formal analysis of these constructs tends to require more effort, making them secondary targets to other blocks described above. If designers consider these factors when selecting the best targets for formal analysis, the resulting ROI tends to be very high.

Methodology

A critical part of the Cadence Incisive formal analysis methodology is to ensure that design and verification engineers apply formal analysis in a way that complements their respective roles.

Designers are in the unique position of having intimate knowledge of the blocks they implement. They understand the intended behavior of the block, its rela-

tionship to other blocks and its implementation in RTL. Therefore, designers are naturally good candidates for writing assertions related to their blocks. Verification engineers, on the other hand, tend to have a better picture of the overall verification plan and the risk areas, and can therefore provide the necessary alternative perspective on correctness.

For designers

The designer can plan for, and aid in, formal analysis. When designing a block or a set of blocks—knowing that data paths and memories can affect the ability to verify control logic using formal analysis—a designer can partition data paths and memories apart from the control logic.

The next step is initial RTL coding and bring-up. Because test vectors are not required, formal analysis is particularly well-suited to block bring-up. In block bring-up, the designer's goal is to get the block to a stage where it mostly works. Initially, a designer focuses on checks that can be extracted automatically, such as lint checks and structural checks.

Designers should write assertions on internal signals that have complex behavior or those they expect to be problematic. Running formal analysis on these assertions will provide an excellent return because failures caught here can be debugged quickly, and failures are very likely in these complex parts of the design.

The next activity centers on checking behavior from a black-box perspective. Here, the designer writes several assertions related to behavior and then checks them using formal analysis. Because these assertions involve many aspects of a design, they can often find subtle bugs due to unforeseen interactions between different parts of the design.

For verification engineers

The verification engineer ensures that the

design works as intended. This means that the individual blocks work correctly and that they work correctly together.

Just as designers must plan for formal analysis early in the design stage, verification engineers must plan for formal analysis early in the verification-planning stage. At this stage, it's important to identify likely targets for formal analysis. Good targets may be areas that are known to have complex functionality or that have had many bugs in other similar projects.

In modern designs, especially system-on-chip designs, blocks are often connected with a few commonly used interfaces. Even within clusters of sub-blocks, a few common interfaces may be used repeatedly. Since these protocols are so widely used within a project, and because ensuring consistent communication between blocks is so important, verification engineers should also develop projectwide or even companywide assertion-based protocol and bus-interface verification components.

Other verification engineers and designers on the team can use these components to verify individual blocks and to speed system bring-up by ensuring that individual blocks communicate with each other correctly. The same verification components can be used by formal analysis, simulation, acceleration and emulation. Because of the multiple ways and places that verification components can be used, creating and using them results in higher ROI for the verification engineer.

Sometimes the verification engineer is in a better position than the design engineer to run formal analysis on a block. For example, when designers are tied up with physical design fixes, they may not be able to devote time to formal analysis. Or, it may be that the verification engineer has been assigned to verify a block and has decided that formal analysis might be the best method.

In those cases, the verification engineer must be able to determine whether the block is suitable for formal analysis and then write assertions, run formal analysis and potentially debug the results. Although high ROI can be achieved, the lack of white-box knowledge makes it more difficult for the verification engineer to determine whether a block is suitable for formal analysis and to debug failed assertions.

Formal analysis may lead to opportunities for savings in verification efforts in other places. For example, engineers may not need to create some directed tests if they understand that verification has already been covered by formal analysis of certain blocks.

Or, if a complex state machine has been verified by formal analysis, then reaching complete coverage for that state machine in the simulation environment might not be necessary. A verification engineer who understands the overall verification plan and understands what parts of the design have been covered by formal analysis is in a good position to assess what other parts of the verification effort can be reduced.

In this discussion we presented a proven approach to achieve high returns with formal analysis. As formal analysis becomes part of mainstream customer production flows, the methodology for adoption and usage plays a key role. When applied in the context of the recommended methodology, formal analysis provides the biggest returns when used early, prior to simulation efforts.

Moreover, both design engineers and verification engineers play important roles in formal analysis use and can benefit from it. With the critical factors in place, the methodology maturing and the ROI clearly defined, this is the ideal time to consider adding formal analysis to your design and verification flow.

Managing multiple evaluations of analog IP

An analog and mixed-signal IP company needs to excel using its creative resources, so it must leverage core skills to produce a growing product portfolio. But with customer evaluations becoming increasingly complex, it is just as necessary to leverage scarce resources in supporting customer evaluations.

Chipidea started with an initial base of high-performance converter technology, then expanded into complete analog front ends and mixed-signal systems, and recently into CMOS RF. Creating reliable, transferable IP in such technologies takes years of knowledge,

hundreds of years of man-effort and a solid understanding of complete systems. But also, vitally, it requires an error-proof approach in design practices and in customer interface and support. And in today's market, the quality of that approach must be demonstrable.

For design, a complete methodology and flow, ISO-certified using a top-down approach, is a must. It is vital to deploy extensive behavioral modeling and full-chip transistor-level simulations and have design steps broken down for added quality control. Chipidea then deploys proprietary data-mining tools and methodologies for result analysis, design tuning and full corner coverage, leveraging automation to improve IP robustness.

Customer interface and support is also important. For example, a "standardized" USB 2.0 OTG PHY that may be certified and fully validated will be available in multiple technologies from 0.18 micron down to 90 nanometers, in several foundries, covering different flavors (generic, low power, etc.). Although similar in functionality, each database will have different implementations. A customer will require silicon characterization results,

certification reports, demo-boards with test chips for the particular process option, reviews and a very reliable support service. The successful IP vendor must be able to show prospects that such a wide range of instances lies within their support capabilities.

An IP company can run lean by leaving out such depth of technology and support. And if prospects do not evaluate their vendors thoroughly, such a company may have short-term success, while harming the image of IP vendors in general. So detailed, in-depth and uniform customer evaluations are to the companies' advantage.

A simple but effective tool like the QIP rating from VSIA will force IP providers to adopt quality procedures, raising market quality and making it easier to evaluate similar cores for the same IP functionality in different processes and flavors. To succeed, one must take all strategies to improve quality and interface. That's why we now rely on the mixed-signal QIP metric from VSIA.

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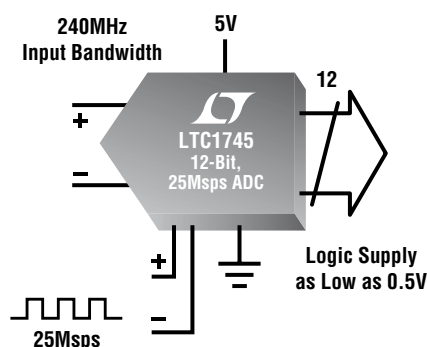


By Carlos A. Leme
(cazeredo@chipidea.com), chief technical officer at Chipidea (Lisbon, Portugal)

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Features:

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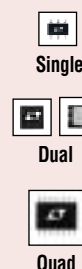
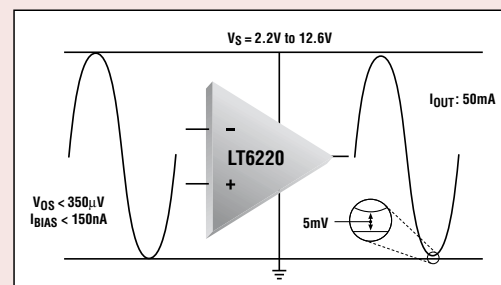


LTC®1745: \$9.30 ea. for 1k pc. qty.

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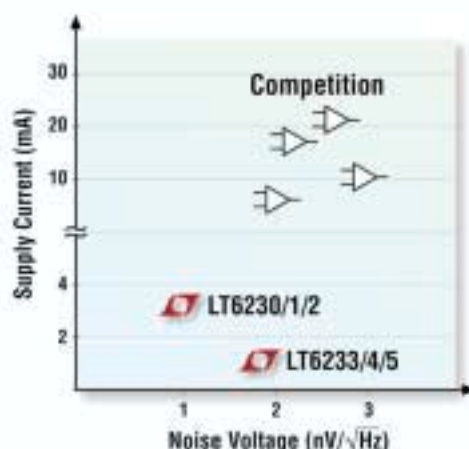
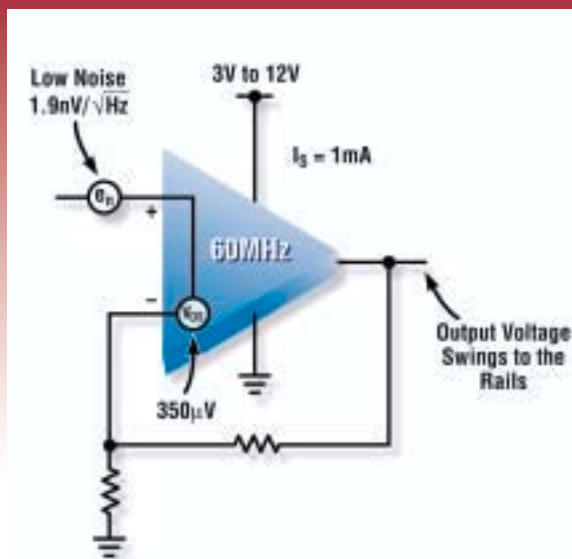
Features:

- Supply Current < 1mA
- Input Offset Voltage: 350 μV Max.
- Input Bias Current: 150nA Max.
- Common Mode Rejection: 102dB
- Power Supply Rejection: 105dB



LT6220: \$1.20 ea. for 1k pc. qty.

1.9nV/ $\sqrt{\text{Hz}}$ Op Amps Draw ~~6.5mA~~ ^{1mA}



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Low Noise Operational Amplifiers

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LT6233-10	1.9	1.05	375 $A_v \geq 10$	115	Out	S	\$1.90
LT6230/1/2	1.1	3.15	215	70	Out	S/D/Q	\$1.25 / \$1.95 / \$3.30
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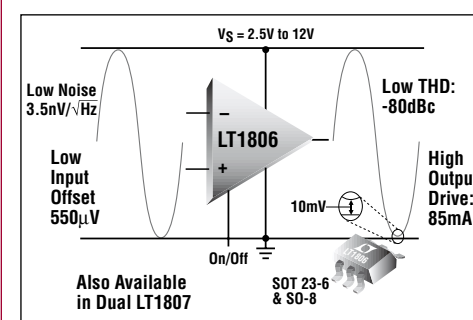
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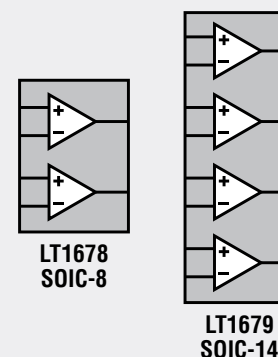


Features:

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- Gain Bandwidth Product: 20MHz
- Supply Current: 3.4mA Max.

LT1678: \$2.50, LT1679: \$3.85 ea. for 1k pc. qty.

Design Currents

TechTrends

Evaluating IP

FROM PAGE 51

to the questions to score well. This latter possibility serves as a warning that just asking a vendor to answer some questions is not going to be enough.

"This is a multistage process," affirmed Philip Dworsky, director of IP applications at Synopsys Inc. "First, it's 'Do they have

what I need?'" Then starts an examination of the vendor's design and verification process. Everybody starts with a different list of questions, but if you pass the initial questions everybody has to go much deeper than paper can take them."

Digging deeper

In fact, the questions on the first-pass checklist may guide further, in-depth assessments as well. "After we have made

the initial decision that a piece of IP is a good candidate for evaluation, we will repeat in-house everything the vendor says he has done," said Jean Bou-Farhat, vice president of the CoWare group at LSI Logic Corp.

"We do a detailed audit to confirm the answers to the questions," said PMC's Harris. "Nobody's going to buy a piece of IP off the Web these days."

For many, the only real proof lies in

shipping silicon—and sometimes, even that isn't enough for experienced IP evaluators. "We try to get silicon validation as early in the process as possible, but sometimes it just isn't available," lamented Cadence's Fazzani. Berman added, "Even when it is available, if the IP block is at all complex, it's unlikely that any one silicon implementation will exercise all of it."

So auditing—in effect, doing a design review with the vendor, retracing its steps and comparing them with your own standards—is vital. This auditing process can be quite invasive, with members of the user team reviewing design flows and—especially—verification flows in detail with the vendor's engineering team. It can, as in the case of Open Silicon, involve discussions with previous users of the IP. And it may involve data that the vendor is unwilling to share or questions the vendor's engineers may find offensive.

But increasingly, as design teams take measure of the risks they are assuming in licensing third-party IP, they are becoming more willing to ask the hard questions. Even with such aids as the QIP Metric, this means an increasing flow of resources into the evaluation process. For this, there may be no solution short of an independent evaluation service—an Underwriters Laboratories for IP, as it were. The VSIA, for one, would love to see it happen, but Kaskowitz is not holding his breath.

"Auditing processes are a first step," Kaskowitz said. "In the long run, it would be great to have an independent certification process. But right now it's hard to see who would fund it."

Thin-and-light

FROM PAGE 56

Dell's Inspiron 600m models compete directly against 14-inch widescreen models from Gateway and HP in retail. At the end of April, these 14W systems accounted for 17 percent of the retail market and 54 percent of the thin-and-light segment. Both Gateway and HP have priced their systems competitively, leaving little wiggle room for profit.

Gateway broke 14W price barriers in January when it launched its 3018GZ—with a Celeron M 1.3-GHz processor, 60-Gbyte hard drive, 512 Mbytes of RAM and a DVD/CD-RW combo drive—for \$999 at Best Buy. HP responded with the comparable Compaq Presario V2205, for \$879.

Both models compete against the Dell 600m analyzed in this article. At prices this low before promotion, manufacturers need to squeeze out as much production cost as possible.

Current Analysis expects to see continued growth in the thin-and-light notebook segment as additional manufacturers bring new systems to the table. The increase in competition, however, will drive prices even lower. Thus we believe that manufacturers with an efficient supply chain, like Dell, will have an edge over their competitors.

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JUNE 22 **Virtuoso Wireless Design Flows—RF IC and System/IC Designs**
11:00 am PDT / 2:00 pm EDT — *Cadence Design Systems*

Today's custom design teams are facing greater market demands, tighter schedule, and ever increasing design complexity and physical effects. Sign up for the Virtuoso wireless design flow webinar and learn about the key elements of an effective wireless design flow and address specific challenges with a methodology that reduces risk in your design techniques. ■

JUNE 22 **Learn How Easy It Is To Build an OS Image With Microsoft Windows Embedded**
11:00 am PT/2:00 pm ET — *Microsoft Corp.*

See how easy it is to build a WE image for your next embedded project. See the steps for analyzing the underlying hardware, configuring, building, downloading and debugging a Windows CE 5.0 and a Windows XP Embedded with Service Pack 2 operating system image. Learn to pre-configure platforms for a broad range of devices and see how using Windows Embedded Studio tools allow you to easily customize any of the over 12,000 components that make up Windows XP Embedded. ■

JUNE 23 **Analog Devices Presents... INTEGRITY RTOS and Blackfin Processors for Security, Reliability Or Time To Market. Who Says You Have To Choose?** — 12:00 pm ET/9:00 am PT
Analog Devices Inc, Arrow Electronics and Green Hills Software

Are your embedded designs secure? Do you worry about your next product being vulnerable to attacks by hackers? This webcast will look at how the royalty-free INTEGRITY real-time operating system takes advantage of the Blackfin architecture, including the Memory Protection Unit, allowing you to build totally reliable, absolutely secure, and maximum performance products—in the least time and with the lowest production cost. ■

JUNE 28 **Analog Devices Presents... INTEGRITY RTOS and Blackfin Processors for Security, Reliability Or Time To Market. Who Says You Have To Choose?** — 9:00 am ET/6:00 am PT
Analog Devices Inc, Arrow Electronics and Green Hills Software

Are your embedded designs secure? Do you worry about your next product being vulnerable to attacks by hackers? This webcast will look at how the royalty-free INTEGRITY real-time operating system takes advantage of the Blackfin architecture, including the Memory Protection Unit, allowing you to build totally reliable, absolutely secure, and maximum performance products—in the least time and with the lowest production cost. ■

JUNE 29 **Performance Clocks: Demystifying Jitter**
2:00 pm ET/11:00 am PT — *Analog Devices, Inc.*

Join us as we delve into the realm of sub-picosecond jitter clocks. The relationship between jitter and phase noise will be explored in detail and methods for measuring sub-picosecond jitter and ultra low phase noise will be discussed. This NetSeminar will cover performance clock IC applications and considerations and the use of ADI's new ADI SimCLOCK clock simulation tool will be featured. ■

JUNE 29 **Retargeting FPGA Designs**
11:00 am PT / 2:00 pm ET — *Lattice Semiconductor*

Development teams are more and more often facing the challenge of retargeting existing FPGA designs. A variety of needs are forcing change including: improved performance, security, component end of life, and system integration. In this NetSeminar, Lattice Semiconductor examines FPGA features that are motivating designers to retarget and provides practical advice for designers who are considering a move from earlier FPGA architectures to cutting-edge, low-cost FPGAs. ■

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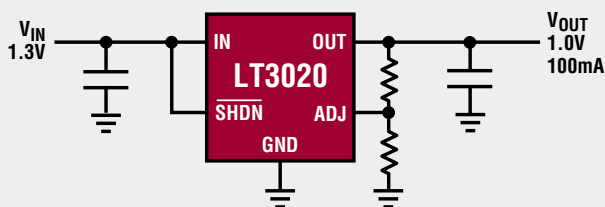
- **PLD Design In a Pb-Free World** — *Lattice Semiconductor*
- **Optimizing Power Consumption In Embedded Systems Using ARM®-Based Microcontrollers From STMicroelectronics** — *STMicroelectronics*
- **Electronics Supply & Manufacturing Editorial NetSeminars: Applying Lean Principles To The New Product Development Process** — *Oracle*
- **TTI Technical Seminar Series: Connectors: The Need For Speed** — *TTI, Inc.*
- **Analog eLab: Utilizing High-Speed ADCs for Undersampling** — *Texas Instruments and Memec/Insight Electronics*
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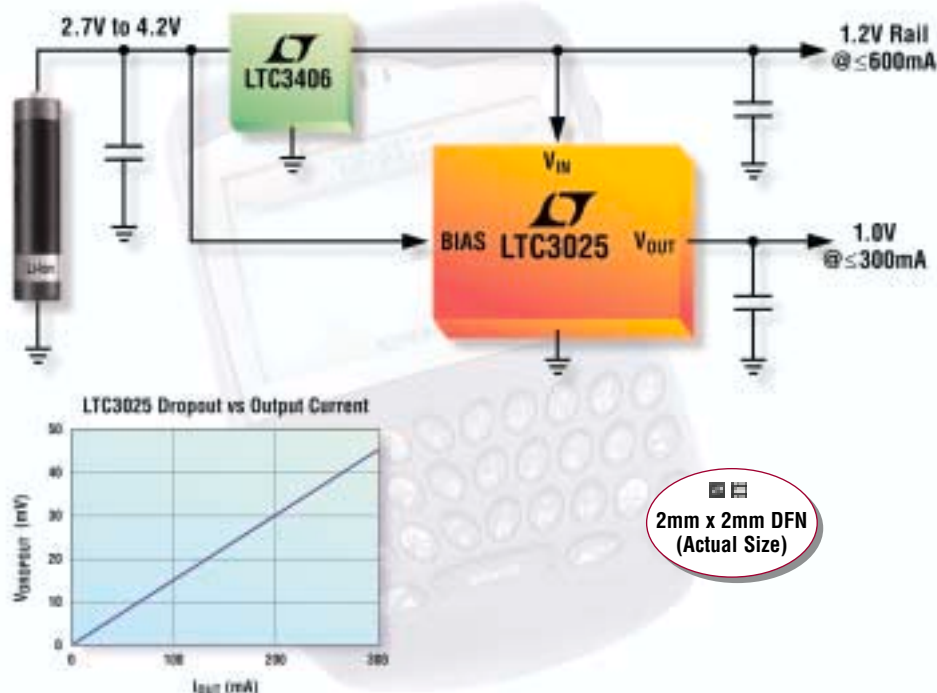
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LTC [®] 1844	150	1.6 to 6.5	1.25 to 6	90	35	ThinSOT™
LTC3025	300	0.9 to 5.5	0.4 to 3.6	45	55	2mm x 2mm DFN
LT3021	500	0.9 to 10	0.2 to 9	150	100	5mm x 5mm DFN, SO-8
LTC3026	1.5A	1.14 to 5.5	0.4 to 2.6	150	400	3mm x 3mm DFN, MSE

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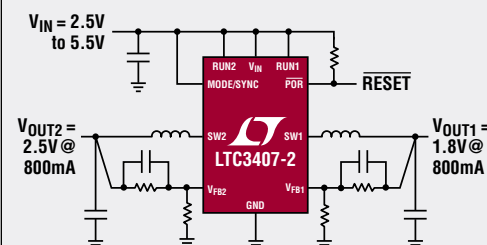
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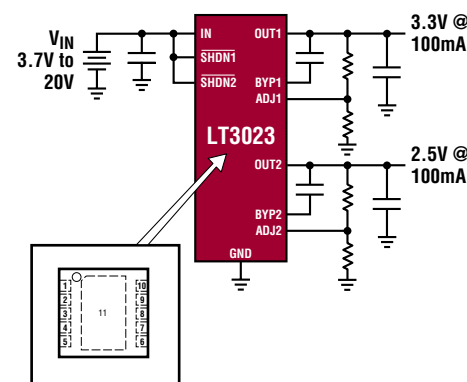
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- Low Power Dissipation: 890mW
- LVDS, CMOS or Demultiplexed CMOS Outputs

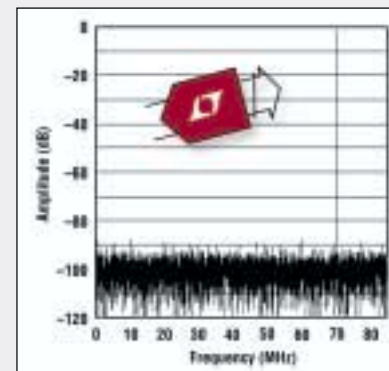


LTC2220-1: \$49.00 ea. for 1k pc. qty.

12-Bit, 170Mps ADC–LTC2220

Features:

- 67.5dB SNR up to 140MHz Input
- 80dB SFDR up to 170MHz Input
- Low Power Dissipation: 890mW
- LVDS, CMOS or Demultiplexed CMOS Outputs



LTC2220: \$39.50 ea. for 1k pc. qty.

Dual Lowest Power High Speed ADCs



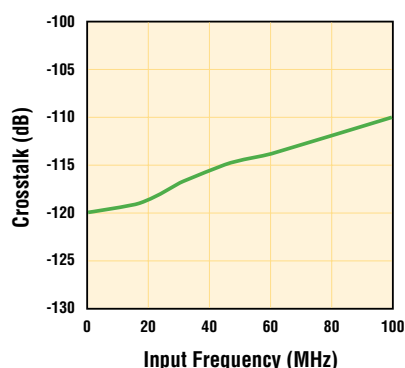
Pin-Compatible Family Features 110dB Channel-to-Channel Isolation at 100MHz

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- 85dB SFDR up to 70MHz
- 110dB Channel Isolation
- Single 3V Supply (2.7V to 3.4V)
- Multiplexed or Separate Data Bus
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Crosstalk vs Input Frequency



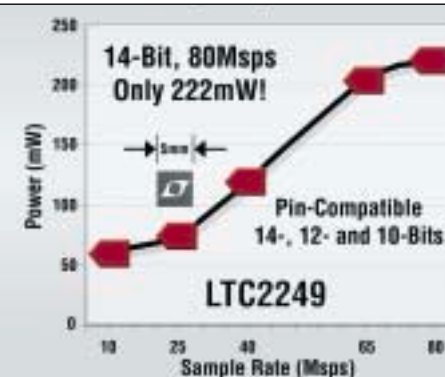
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14-Bit, 80Mps ADC–LTC2249

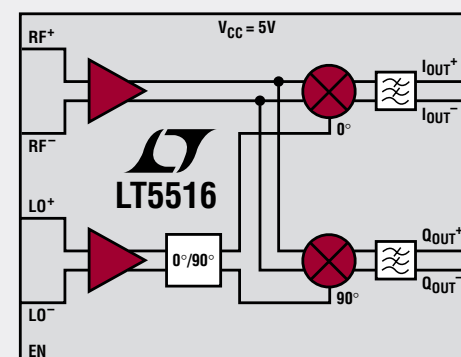


Features:

- Single 3V Supply (2.7V to 3.4V)
- Low Power: 222mW
- 73dB SNR at 70MHz Input
- 90dB SFDR at 70MHz Input

LTC2249: \$25.00 ea. for 1k pc. qty.

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PRODUCT OF THE WEEK

Atmel ratchets 10-bit A/D clock to 2.2 Gsamples/s

Device targets applications in broadband test, telecom, defense

By Bettyann Liotta

San Jose, Calif. — Atmel Corp. says its 10-bit analog-to-digital converter, with a clock frequency of 2.2 Gsamples/second, is one of the fastest in the industry. The AT84AS008GL is pin-compatible with Atmel's TS83102G0BGL and older, 2-Gsample/s 10-bit A/D converter.

The new A/D converter provides a full 8 effective number of bits at 1.7 Gsamples/s in first Nyquist. The unit targets such high-speed digitization applications as broadband test and measurement equipment, high-speed data acquisition, telecommunications and defense.

The AT84AS008GL is the latest in Atmel's family of gigahertz 10-bit data converters. It provides a new level of linear performance over first and second Nyquist zones while reducing power consumption and improving frequency spectral response.

The converter offers dynamic performance of 55-dB spurious-free dynamic range (SFDR) and 51-dB signal-to-noise ratio (SNR) at 2.2 Gsamples/s in first Nyquist conditions, according to Atmel. Furthermore, the 3.3-GHz input bandwidth extends A/D converter operation well into the second Nyquist zone with essentially flat performance: SNR remains at 48 dB and SFDR at 55 dB.

A new Atmel companion demultiplexer chip, the AT84CS001TP, lets users interface the AT84AS008GL with FPGAs, DSPs or ASICs. It

CONTINUED ON PAGE 70

Cable assembly aims at speedy backplanes

Elkton, Md. — Leveraging their respective expertise in cable and interconnect technologies, W. L. Gore & Associates Inc. and FCI have partnered to offer the next generation of high-data-rate digital interconnect solutions.

The cable assemblies leverage the advantages of FCI's AirMax VS high-speed connection system with Gore's expertise in cable

bit/second using only 50 linear millimeters of backplane space, said David Gioconda, global data communications market segment leader for Gore.

The cable assembly consists of cable using Gore's expanded polytetrafluoroethylene (ePTFE) as the dielectric core. The helically wrapped ePTFE core ensures constant impedance throughout the

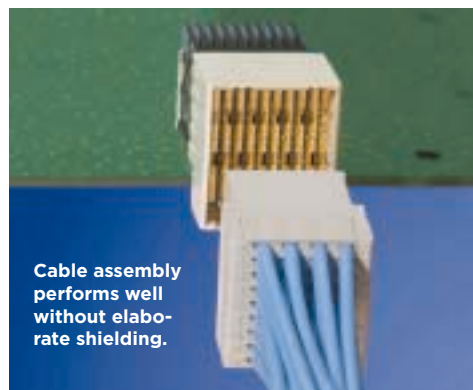
length of the cables with excellent stability with temperature cycling or flexing, the company said.

The cables also exhibit low signal loss, low crosstalk, low skew and controlled capacitance and controlled impedance to provide the most open eye patterns available at this density. Available in differential or coaxial cable configurations, impedance is

rated at 100 ohms $\pm 5 \Omega$ for differential and 60 Ω nominal for single-ended configurations.

Priced at \$1/gigabit per meter, the Gore high-density copper cable assemblies are available in a number of standard configurations. Call (800) 445-4673

Search www.eeProductCenter.com for article ID: 163701838

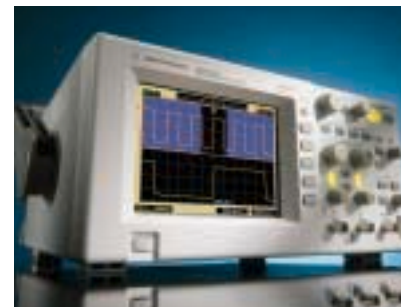


assembly development. The new configuration uses the patented AirMax connector concept to provide the high-frequency performance without elaborate shielding. Applications include telecommunications, large-scale computing and automatic test equipment.

The data link can provide an aggregate bandwidth of 1 tera-

Oscilloscopes

By Alex Mendelsohn



Agilent's DSO3000 packs color VGA LCDs, offers flexible triggering features.

Feature-rich 'value' scopes suit many apps

It doesn't make economic sense to equip an engineering lab bench, a field technician's tool kit or a school lab with a high-speed, expensive oscilloscope when a 60-MHz or 100-MHz instrument will fill the bill. Just think how many systems designers and troubleshooters require oscilloscopes that can reveal the waveforms of lower-speed logic, slow microcontroller signals, audio and lower-frequency RF signals, motor control signals and the like.

That's where low-bandwidth but feature-rich oscilloscopes fit in. These instruments serve the so-called value user, much as value notebooks serve mainstream cost-sensitive PC users.

Agilent Technologies Inc. offers portable digital-storage oscilloscopes with bandwidths of 60, 100, 150 and 200 MHz. The DSO3000 series epitomizes the concept of a dual-channel value scope, but these instruments, like today's notebook PCs, pack a lot of bang for the buck.

Equipped with big color LCDs, Agi-

CONTINUED ON PAGE 68

REVIEW OF THE WEEK

Supercapacitors shoot for penny/farad pricing

Maxwell touts improvements in Boostcap cells, modules

San Diego — Maxwell Technologies has launched the first of a family of large-cell Boostcap ultracapacitor cells and multi-cell modules based on technology that lets them store more energy, deliver more power per unit volume and last longer than other commercial ultracapacitors.

Richard Smith, Maxwell's executive vice president for strategic business development, said the just-released, 2.7-volt Boostcap MC2600, a 2,600-farad large cell, and the fully integrated BMOD2600-16 16-V module, incorporating six MC-2600 cells, "meet or exceed automotive



Maxwell claims longer life and more power per unit volume for its Boostcap large-cell family.

REVIEW CONTINUED ON PAGE 74

eeProductCenter's Vincent Biancomano offers his review

With its latest announcement, Maxwell Technologies implies that there is an inflection point in the cost/volume curve that's critical to the successful development and production of the supercapacitor. "We must be at half a cent per farad by 2010," said Robert Tressler, senior vice president of sales.

The company's MC2600, at 1 cent per farad in high numbers (annual volume of 1 million units) and with a production volume expected to approach 100,000, goes a long way toward meeting that goal.

An improved electrode system and bet-

➔ For more details on these and other new products, visit our Web site: www.eeProductCenter.com. Each week, our editors pick the best and most exciting products in 16 categories, from power management to DSPs. If you have a product to submit, please e-mail mgold@cmp.com.

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Test

Low-end scopes

FROM PAGE 67

lent's dual-channel sampling scopes are priced from less than \$1,000 to about \$1,900. That puts them squarely in the domain of mainstream probing. The scopes include 320 x 240-pixel VGA LCDs, an array of triggering capabilities and the

ability to make automatic measurements. They have 1-Gsample/second sampling rates, 4,000 points of waveform memory, digital filtering, four math functions and sequential memory acquisition. The sequential memory mode makes it possible to frame an area of interest on a signal and then get a playback that lets you quickly look through a sequence to spot glitches or anomalies. The DSO3000 series can also to crunch through fast Fourier transforms to enable spectral analysis of waveforms.

The low-cost scopes can also communicate in automated test suites, thanks to IEEE-488/GPIB, RS-232 and USB connectivity options. Those hooks can link to PCs for documentation or spreadsheet analysis.

The scopes support USBTMC-USB-488 transfers at 10 Mbytes/s. USBTMC-USB488 also lets the user control a 3000 series oscilloscope via an optional software package. (For more details, search www.eeProductCenter.com for article ID: 160903619.)

Competitors Fluke Corp. and Tektronix Inc. also offer feature-laden, low-cost oscilloscopes. Recently, both companies dished up portable scopes for industrial users.

Fluke's Power Quality Division now has a line of ergonomically crafted low-cost scopes tailored for three-phase power quality analysis. Instruments in the 430 series are priced at about \$3,500 and are rated to CAT III (1,000 volts) and CAT IV (600 V) for all four channels.

The instruments let users perform power quality testing at service entrances and other industrial wiring locations. Thanks to the units' safety rating, Fluke's 430 series can measure all phases, neutral and ground, on virtually every connection in a low-voltage electrical distribution system, the company said. Measurement capabilities encompass true-rms voltage and current, frequency, power and energy. The scopes can also help determine causes of unbalance, flicker, interruptions, rapid voltage changes, dips and swells. They automatically capture transients as fast as 5 μ s and as high as 6,000 V.

The Fluke scopes' AutoTrend feature automatically records everything on screen. Likewise, Fluke's System-Monitor feature helps technicians and semiskilled personnel perform quick diagnoses of system performance against user-defined limits. Users can even view stored data while continuing to record.

Together, the features help to quickly diagnose problems and build benchmarks for predictive maintenance, according to Fluke. (Search www.eeProductCenter.com for article ID: 51202441.)

Tektronix's latest TPS2000s compete with Fluke's portable scopes. But unlike Fluke's ergonomically designed

handhelds, Tek's oscilloscopes look more like conventional bench instruments, albeit thinner and smaller.

Like the Fluke scopes, Tek's instruments make power-specific measurements on four isolated channels simultaneously. They also supply a familiar front panel, with independent knobs and buttons for each channel.



Tektronix's battery-powered scopes provide high sampling rates and have quarter-VGA color displays.

Industrial-power users often work on devices that are floating or have different grounds. Such users need to measure high voltages and currents. They often also need to validate control logic that's associated with the power circuits. In those cases, what's needed is a scope that can provide accurate performance on up to four channels simultaneously.

What's more, they need an instrument that can move among the benchtop, the power lab and the field. The TPS2000 models address those needs with four iso-

lated channels in a battery-powered package. Tek's IsolatedChannel technique supports both grounded and floating high-voltage measurements, such as those found in three-phase power circuits with different low levels or ground references.

The TPS2000 units also offer Autoset menus for waveform selection. These ensure fast isolation of events of interest and the ability to leverage a host of triggering options, including triggers to lock onto signals in mixed-signal environments, the company said.

Like Agilent's offerings, Tek's portable scopes can be used to perform device characterization using automatic measurement. Automatic waveform measurements include those for a signal's period, frequency, width, rise and fall times, maximums/minimums, and peak-to-peak and mean values.

A standard feature on all of Tek's TPS2000 scopes (and only included on Fluke's 190C model) is the ability to do an FFT on waveforms to look at signals in the frequency domain. That can help reveal signal interference, crosstalk and the effects of vibration, Tektronix said. FFT operation is more or less a standard feature on many scopes these days; it's significant that Tek includes it on an industrial-oriented product line.

Tek's scopes tout high sampling rates and quarter-VGA color displays. The TPS-2012 is a dual-channel 100-MHz scope with a 1-Gsample/s rate that's priced at less than \$3,000. The TPS2024 four-channel, 200-MHz instrument, featuring 2-Gsample/s sampling and a 200-MHz bandwidth, sells for about \$3,800. In between, Tek is offering its TPS2014, a four-channel, 100-MHz box with a 1-Gsample/s rate. It's priced at about \$3,400. (Search www.eeProductCenter.com for article ID: 47101936.)

For the full text, search www.eeProductCenter.com for article ID: 162100628.

TDR instrumentation uses Universal Serial Bus port

Beaverton, Ore. — These days, more and more lab instruments are powered and operated through a PC's Universal Serial Bus port. A new product from time-domain reflectometry equipment supplier HyperLabs is a case in point. The company's TDR instrumentation line, which already is expansive, now includes a Model USBTDR family of so-called TDR heads that are powered by USB.

The company's Model HL8200USB, priced at about \$3,300, provides 200-picosecond rise time signals to measure discontinuities in transmission lines as close as 4 centimeters on cables as long as 400 meters in length. In use, the module generates a 250-millivolt stimulus voltage step on its SMA coaxial cable out-

put connector. It then takes samples from the incident pulse and the signal reflected from the device under test.

The instrument's vertical scale is selectable in mV, reflection coefficient, and a normalized or direct impedance reading.

Such high-resolution TDR instruments are useful in the characterization of components, interconnects, backplanes, and circuit boards used in multi-GHz clock-rate PCs, as well as Gbit differential communication systems.

The Model HL1100USB is priced at about \$5,700 and the Model HL2200USB at about \$7,700.

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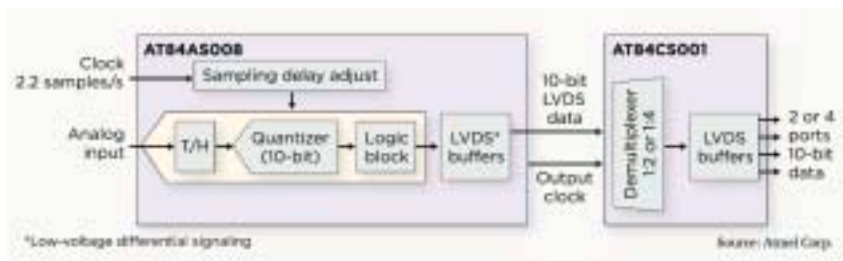
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A/D-demultiplexer combo enables 2.2 Gsamples with 1:4 or 1:2 LVDS-compatible demux ratios.

10-bit A/D

FROM PAGE 67

provides 10-bit, 2.2-GHz performance with 1:4 or 1:2 low-voltage differential-signaling (LVDS)-compatible demultiplexing ratios. The demux chip operates at data rates of up to 550 Msamples/s.

In addition, the fast Fourier transform spectral response remains very stable over temperature and clock frequency variations, allowing significant system performance enhancement through digital processing even under severe environmental conditions, the company said.

The A/D converter comes in a CBGA

152 ceramic package and operates over commercial and industrial temperature ranges. A military-grade version is planned for 2006. Samples are available now with production quantities slated for next month.

Pricing, availability

In 1,000-piece quantities, pricing is \$1,100 each for the AT84AS008GL.

Also available for sampling now is the AT84CS001TP demultiplexer chip, priced at \$220 each in the same quantities. Volume production will begin this month.

Call (408) 451-2855

Search www.eeProductCenter.com

for article ID: 164301117

Class D amp designed for use with flat panels

Dallas — A digital-input Class D audio power amplifier from Texas Instruments Inc. is said to enable the development of flat-panel displays with sound quality that matches the display's high-quality image, while minimizing cost and component count.

Suited for 27-inch and larger FPDs, the amp operates more efficiently than traditional linear amplifiers, minimizing heat and eliminating the space required for an external heat sink, said Eric Droge, TI's marketing manager for audio power amps. It also minimizes overall power consumption.

The amplifier operates from 8- to 18-volt supplies and has less than 1 percent (0.09 percent at 1 kHz) total harmonic distortion plus noise at half the rated output power and less than 10 percent THD+N at the maximum rated output.

"The operating voltage range includes 12 V, which is a common supply rail in flat-panel displays. And the ability to operate up to 18 V provides

enough voltage swing on the outputs to drive 20 watts at 10 percent THD+N or 10 W with 0.09 percent THD+N," Droge said. Features include three integrated gain settings, power supply rejection ratio of -60 dB, thermal and short-circuit protection, and power-saving shutdown mode. No D/A converter is required.

The 250-kHz switching frequency oversamples the audio signal a minimum of 10 times to ensure high-quality audio that is equal to or better than the linear amplifiers used in flat panels today, according to Droge. The amplifier's digital 24-bit Inter-IC sound (I²S) or 16-bit right-justified input connects directly to most audio processors.

The TPA3200D1 is available in volume in a 44-pin TSSOP. Pricing in 1,000-piece quantities is \$2.95. An evaluation module is available.

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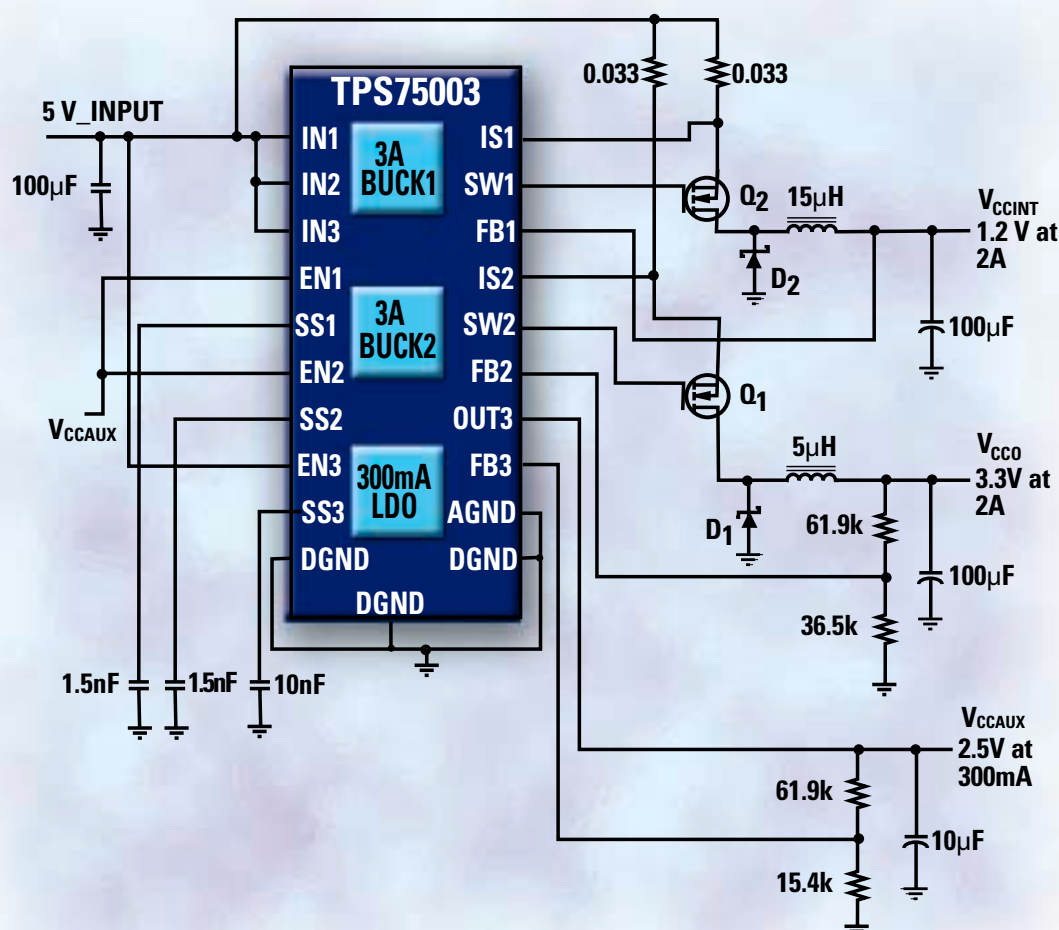
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For more information on TI's complete line of power management solutions for Xilinx FPGAs—including a library of reference designs, schematics and BOMs—visit www.ti.com/xilinuxfpga-u.



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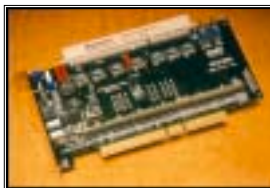
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Power Products

PWM controller saves power at every turn

Santa Clara, Calif. — National Semiconductor Corp.'s LM5021 pulse-width modulation controller contains the power-saving features designers need to build energy-efficient single-ended flyback and forward ac/dc converters for telecom, networking, and industrial and consumer power supplies, the company said.

The PWM controller integrates a high-frequency current-mode design (for improved transient response and simplified loop compensation) with internal slope compensation (LM5021-1 only) to protect against subharmonic oscillation at duty cycles greater than 50 percent. It has user-programmable soft-start and a 0.7-amp MOSFET driver and includes skip,

burst and low-power bias circuitry to boost efficiency over a wide load range.

The LM5021 is available in two versions, distinguished by the maximum duty cycle of its pulse-width modulator—80 percent (LM5021-1) and 50 percent (LM5021-2)—to cater to flyback and forward converters, respectively. Available in MSOP-8 and MDIP-8 packages, the LM5021 is priced at 45 cents each in quantities of 1,000. All packages are available lead-free. A data sheet is available at <http://cache.national.com/ds/LM/LM5021.pdf>.

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Search www.eeProductCenter.com for article ID: 163702831

Extended range UPSes field industrial, telecom apps

Chicago — Tripp Lite's three-phase SmartOnline uninterruptible power supplies (UPSes) extend to the 20- and 30-kVA region for computing, networking, telecom and industrial uses.

The true double-conversion systems' power module includes an inverter/charger section (less than 3 percent total harmonic distortion at output), three communication ports as well as an SNMP slot.

The suggested retail prices for the SU20K3/3 and SU30K3/3 systems are \$14,399 and \$23,519, respectively. The company also offers SmartOnline models for the 10- to 30-kVA international market. These models include the SU10K3/1X, SU20K3/3X and SU30K3/3X parts.

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Search www.eeProductCenter.com for article ID: 162800029

REVIEW OF THE WEEK

FROM PAGE 67

Maxwell's release

requirements for both watt-hours of energy storage and watts of power delivery per kilogram." The cells "will perform reliably for more than 1 million discharge-recharge cycles at 2.7 V, he said, and "the proprietary technology on which they are based reduces material and production cost, positioning Maxwell to achieve our goal of pricing large-cell ultracapacitors at 1 cent per farad in million-cell annual volumes."

The cylindrical MC2600 cells, constructed of lightweight aluminum and Maxwell's proprietary electrode, measure 138 mm in height and 57.7 mm in width. Weight is 470 grams. They feature a double-ended design that is available in two versions, to facilitate either mechanical or welded termination. They are priced at \$54 per cell in midrange volumes.

The BMOD2600-16 modules are encased in a splash-proof aluminum chassis. They weigh 5 kg and are less than 4.85 liters in volume. Temperature and voltage monitoring and internal cell balancing give designers "plug and play" solutions, and module-to-module balancing makes them versatile building blocks for systems with higher voltage requirements. They are priced at in midrange volumes.

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eeProductCenter's review

ter mechanical construction overall take credit for most of the gains for this double-layer capacitor. "First, we've brought the cell rating to 2.7 volts, compared with the 2.5 V it was previously," said Bobby Maher, director of technical sales for the Boostcap line. "That 8 percent increase means fewer capacitors for a given application, and the cost of a system is directly related to the cost of the cells."

"The device is also specified for a million charge-discharge cycles. At the same time, we've decreased size by 14 percent."

In terms of power density and energy density, that equates to 10.4 kilowatts per kilogram and 5.6 watt-hours/kg, respectively. The supercaps are rated for operation over -40°C to $+65^{\circ}\text{C}$.

The improved performance is tied to the device's reduced internal resistance. In this case, it's 0.4 milliohm per cell, about a 40 percent improvement over the current-generation BCAP0010 (0.7 milliohm). Moreover, the spec is the capacitor's dc internal resistance, vs. the internal resistance at low-frequency ac.

In the typical application, the designer will draw greater advantage from the low-resistance design that comes in the device's laser-welded package than from a second version of the MC2600 package. The latter version has threaded-terminal interconnects, suitable for those just getting acquainted with a basic power backup/bridging application.

For the complete text of this review, please search www.eeProductCenter.com for article ID: 164300055

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News

Beyond the Horizon

U.S. broadband

FROM PAGE 20

mixing broadcast overlay and IPTV models, but we have to assume that a single home platform must support multiple streams of multicast IP traffic," Aalaei said. "When I say 'triple play,' I can't refer to support for a single broadcast channel."

In general, PON semiconductor makers are either following the ATM-oriented evolutionary path of APON to broadband PON and then gigabit PON or are leaping straight to the Ethernet-only EPON and GEPON environment (the approach favored in some Asian nations). BroadLight Inc. and Freescale Semiconductor are high-profile GPON suppliers; Teknovus Inc. and Passavé Technologies have cast their lot with EPON.

At the end of the day, the real issue is how packetized services are handled. That means VDSL/VDSL2, or even ADSL2+, can be used as a temporary last-mile feeder for PON service; but, long term, PON must extend deeper into the network toward the end user.

"If I have a copper infrastructure I want to utilize, it may make sense to have a

fiber-to-the-node architecture that uses VDSL or VDSL2," said Matt James, senior marketing manager for PON products at Alcatel North America. "But when service providers want to address IPTV, they have to look seriously at a network transformation."

"Yes, you can do true triple play with VDSL2, maybe even with the 26 Mbps/second of VDSL1, but you'll need GPON to the premises for speeds above 100 Mbps a second—and I think that is the end game most aim at."

Juniper Networks believes the optimal TV delivery mechanism for carriers using PON will be to put broadcast channels and a standard cable package on an independent wavelength, using an overlay model without a TCP/IP stack. Custom channels chosen by the individual consumer then would be delivered via streaming IP TV. Boland of Juniper said the approach would yield most of the features of the multihundred-channel environments that Japanese carriers are delivering via active fiber, but without the heavy bandwidth requirements of switched active fiber.

Niket Jindal, program manager for PON at Freescale, said such an architec-

ture may be compelling, but "every time you talk about an RF video overlay, there are costs associated with distinguishing different types of TV delivery. Ultimately, we need to get fiber all the way to the home, and eventually there may be more active fiber components in the network."

At the same time, Jindal said, "we cannot look too closely at Asian markets with dense populations as models. First of all, there's a lot less focus in the U.S. on upstream speeds than in many Asian markets. Second, with a large and distributed population in the U.S., network evolution always takes longer than we anticipate."

Taking on too much?

Is a shift from ADSL2+ to VDSL2 perhaps too big a jump for networks with copper extending from optical network nodes? Tony Zarola, strategic business manager for broadband products at Analog Devices Inc., noted that DSL customer-premises equipment manufacturers have just upgraded to the 24-Mbit/s ADSL2+, so expecting them to migrate now to VDSL2 may be asking too much. A better option may be bonded ADSL2+ channels, Zarola said. In bonding, two channels are log-

ically combined to provide the aggregated bandwidth of the two channels. Thus, two 26-Mbit VDSL1 bonded channels would provide the equivalent of more than 50 Mbps/s.

Infineon Technologies Inc., for its part, is betting that the bonding option will prove just as viable for VDSL2, where it would provide consumers the same 100-Mbit speeds they could get from active-fiber connections.

Tom Starr, chief standards director at SBC, said carriers regard VDSL2 as a breakthrough for complementing passive fiber strategies that move to the neighborhood. Starr, who had worked on various DSL standards, said the work to finish VDSL2 has generated more excitement than he has seen since "at least the very early days of ADSL."

The newest use of DSL comes from Aktino Inc., a startup founded by PairGain Communications executives that uses multiple-input, multiple-output frequency division multiplexed channels for copper binding. The company launched backhaul and metro-extender roles for its MIMO-over-DSL system, based on T1/T3 channels, in early May and showed an Ethernet version of the same system at the Supercomm show.

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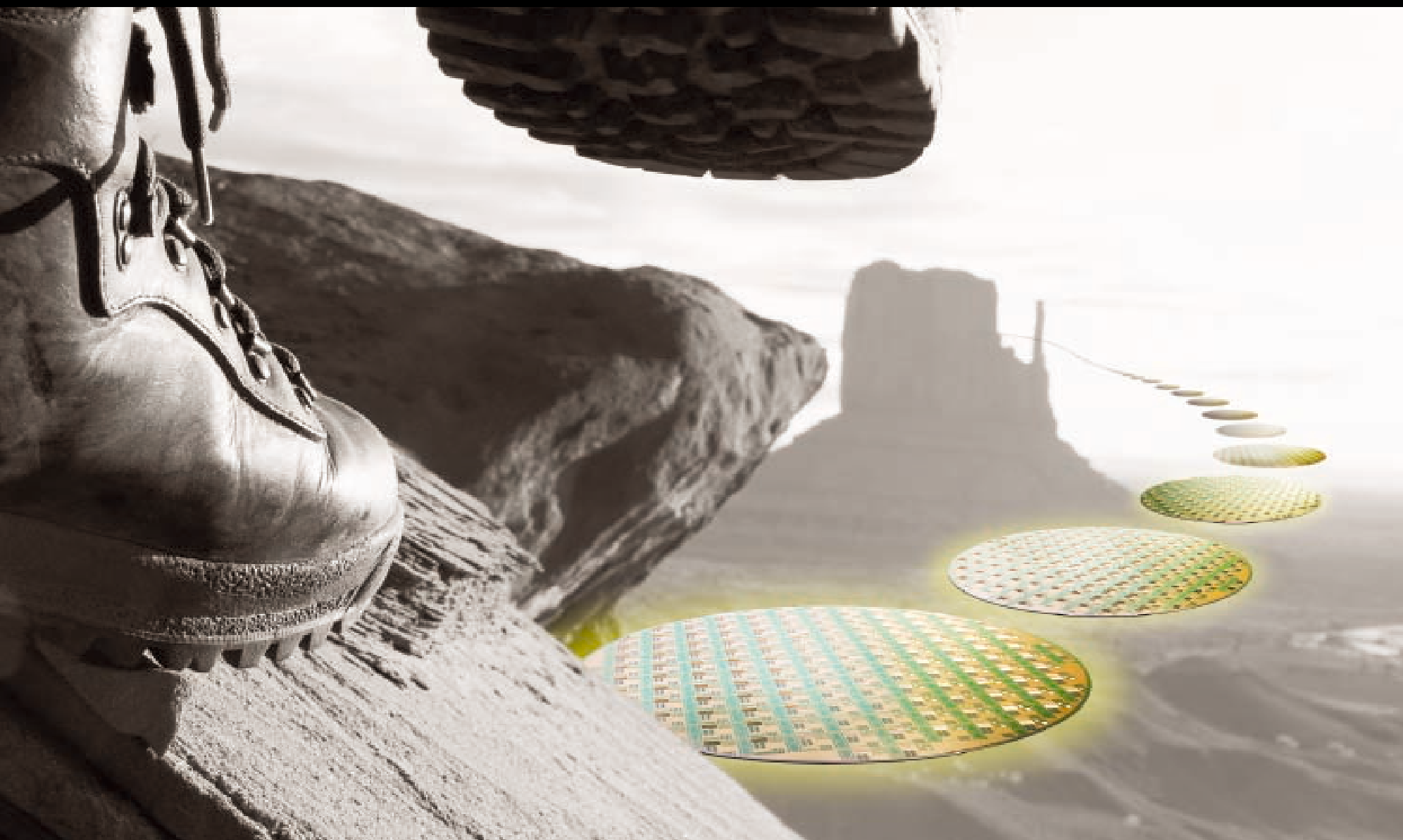
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Accelerating Silicon Success

News

China's IC gear bid

FROM PAGE 1

and 6-inch fabs. Because modern semiconductor fabs are still relative newcomers to China, the country's nascent equipment industry has not done much in the areas of advanced semiconductor tools and materials.

But that is beginning to change as a handful of domestic startups quietly develop tools. Though most of the efforts thus far have been in chemical vapor deposition (CVD) and etch, a couple of companies and government labs are exploring more-advanced lithography. Little is known about the startups, which generally eschew the spotlight, but industry observers believe a few of them have potential staying power.

The nation's fledgling semiconductor equipment industry "could serve markets not addressed by Applied Materials, Lam Research and others, but what I'm worried about is patent protection," said analyst Avinash Kant, who follows the IC-equipment market for investment banking firm Adams Harkness Inc. (Boston).

"Most of the technology [in the semiconductor-equipment industry] is already patent-protected," Kant said. "It's hard to get around these patents. But in China, patents are not protected."

China's domestic equipment market is one of the fastest-growing in Asia, weighing in at \$2.6 billion in 2004, up 132 percent from 2003. Growth is moderating this year as the country's biggest foundry, Semiconductor Manufacturing International Corp. (SMIC), curbs spending.

However, over the long term, observers expect China to be a magnet for companies building fabs, thanks to tax incentives and subsidies and to the growing electronics supply chain here. Twenty new fabrication facilities will be constructed in China between 2005 and 2008, the Semiconductor Equipment and Materials International (SEMI) association reported this month.

"In the next couple of years, the demand for low-priced equipment will grow based upon the current announced 200-mm fab projects. Local vendors may be able to come in with low prices and compete with secondhand-equipment vendors," said Mark Ding, president of SEMI China. "More 300-mm fabs are in planning in China, which gives the local vendors the opportunity to grow into higher-margin areas if they do well in supplying 200-mm equipment and keep up with the R&D."

In Shanghai, a group of former Applied Materials executives appears to be a front-runner. The executives form the core of Advanced Micro-Fabrication Equipment Inc. (AMEC), which is developing CVD and etch tools and should have prototypes by the end of this year, with market-ready

systems available in 2007.

The company's game plan, which calls for 30 percent market share in Asia by 2012 to 2015, is admittedly aggressive. But the plan proved intriguing enough to attract \$38 million in venture capital and the attention of Lip-bu Tan, an early investor in Chinese foundries SMIC and Central Semiconductor Manufacturing Co.

Tan, of Walden International, led the investment in AMEC by a group of Silicon Valley firms: Redpoint Ventures, InterWest Partners, Lightspeed Semiconductor and Bay Partners. The investment arm of the Shanghai government chipped in \$6 million.

AMEC is still in stealth mode and thus isn't divulging its product plans yet, said venture capitalist Koji Osawa, a "board observer" of AMEC. Osawa is a principal and co-founder of venture capital firm Global Catalyst Partners (Redwood Shores, Calif.), which invests in AMEC and other companies.

China's semiconductor companies are looking for low-cost equipment alternatives to their foreign rivals, and the fledgling Chinese tool vendors could one day become a viable source of supply in select product markets, Osawa said. "It's not a well-developed market right now, but I think China's equipment vendors have a chance to get into this space," he said.

But soaring development costs, coupled with stiff competition from foreign rivals, could limit China to just a few fab-tool vendors. "I don't see that many equipment companies in China," Osawa said.

China currently is home to about 40 domestic manufacturers of equipment for the semiconductor and related micro-electronics industries, according to SEMI. But few of those pose an immediate threat to overseas rivals; most are either in back-end equipment or are serving legacy 4-, 5- and 6-inch fabs, which consume more than half of the silicon in China.

"The industry in China is still quite young, and companies won't be coming out with anything for some time," said an executive at an equipment startup in China who requested anonymity. "But China would like to establish a semiconductor industry, and equipment is the foundation of that industry."

Local companies have been lobbying the government for some time to spend more money on R&D for advanced equipment, and the government seems keenly interested in speeding development of the local chip and LCD equipment industries. It wants to encourage fabs to buy domestic machinery, but any policy would have to be carefully crafted so as not to run afoul of World Trade Organization rules,

as an older tax-rebate policy did. One possibility is routing R&D funds to both foundries and local equipment makers, which could come together under a group similar to Sematech.

Such activity, if duly supported by China's chip makers, could foster a stable local supply of advanced equipment, avoiding the sticky issue of foreign-export licenses for tools that can make chips for basebands as well as missile-targeting systems. And it would introduce more competition into the market, driving down prices.

Opinions are mixed about whether China will become a force to reckon with in the semiconductor equipment and materials market. Market leaders like Applied Materials and ASM Lithography don't see an immediate threat, but they're

Corning (Midland, Mich.). "I don't see any photoresist companies in China. I don't see any CMP slurry vendors."

Dembowski believes China-based equipment companies could succeed in selling into the domestic market but not to the markets in other Asian countries, Europe or the States.

But that's exactly what AMEC and others, such as

Shanghai Micro Electronics Equipment and Beijing Seven Star, intend to do eventually. They hope to persuade local companies to start testing their equipment, perhaps during a downturn, when process engineers might have more time. They believe that their products' lower cost of ownership—in some cases, as much as 35 percent—plus promised performance advantages will compel both foreign and domestic companies to take a chance on them.

It will take a while. South Korea has been trying to build up a strong equipment industry since the late 1980s, but it's stalled out at about a 10 percent to 15 percent global market share. Taiwan has tried, too, but with poorer results.

Still, there's room in the market for standouts. One of the fastest-growing companies in the equipment business is South Korea-based Jusung Engineering Co. Ltd., a provider of semiconductor and LCD manufacturing tools. It has gained the confidence of customers in Asia, the United States and Europe, boosting revenue from 27.1 billion won in 2003 to an estimated 223.7 billion won in 2005.

Japan has been Asia's biggest equipment success story; yet, even there, companies cloned existing equipment before moving on to their own innovations. Chinese companies can likewise be expected to do some copying. And China's lax IP laws could make it difficult for international competitors to take action.

A better way for companies to protect their market share may be to emphasize the extras, such as integration and after-sales service. Big vendors will have a clear advantage in working more closely with the fabs, especially those in China and Taiwan that may need more integration assistance or that want closer collaboration on process development.

"A lot of times, it's very difficult to make that competitive jump from copying something to actually providing a solution that works at the customer site," said Dan Hutcheson, president of VLSI Research Inc. (Santa Clara, Calif.), an equipment industry specialist.

For China, the bottom line is that it is home to an industry in its infancy—and a customer base that's smaller than Japan's and not as vertically integrated as South Korea's. Those will be handicaps to overcome.

"It's probably a long haul for them, maybe 10 or even 20 years before it is a viable business," said Hutcheson. "But remember, the Chinese are very patient."

'The U.S. will have to be more competitive than we are today.'

China needs more wafers

Estimated annual silicon wafer consumption

	2003	2004	% change
≥100 mm	2,250,000	2,750,000	22%
125 mm	880,000	1,150,000	31%
150 mm	1,610,000	2,780,000	73%
200 mm	860,000	1,700,000	98%
300 mm	NA	NA*	—

*China's first 300-mm fab began pilot production in 2004

Source: Semiconductor Equipment and Materials International

concerned about the outlook five years down the road.

"I think China will build equipment," said Jim Easton, vice president of sales and marketing for Silecs Inc. (San Jose, Calif.), a low-k dielectric materials startup. "That will require the United States to become more competitive than we are today."

The fab-tool industry in China "will pick up very fast," predicted Werner Rust, senior director of sales and marketing for ASM NuTool Inc. (Fremont, Calif.), part of Netherlands-based ASM International BV. "It will take three to five years."

Rust said he doubts Chinese companies will be able to develop a complex technology like optical lithography all that quickly, but he believes some could move into niche markets. "They will start out and build their own furnaces. I am sure they can build vacuums," he said. "I don't think they will go out and develop atomic-layer deposition, but I could see them doing CMP [chemical mechanical polishing]."

More important than the physical plants, China is building up the know-how. A growing number of Chinese nationals who once worked for U.S.-based equipment makers are now nurturing the nascent domestic industry, according to Rust.

Others are not as optimistic about China's fortunes in the sector. "They are slow and behind in materials," said Philip Dembowski, global market manager for semiconductor fabrication materials at Dow

'China wants a chip industry, and equipment is the foundation.'

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Operating Voltage	RAM Retention	Standby Real-Time Clock	
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