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ISSUE 1374

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MONDAY, JUNE 6, 2005

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TOC



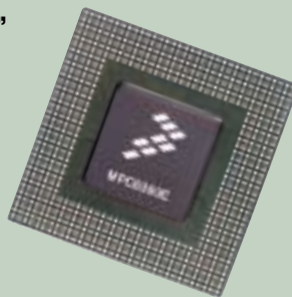
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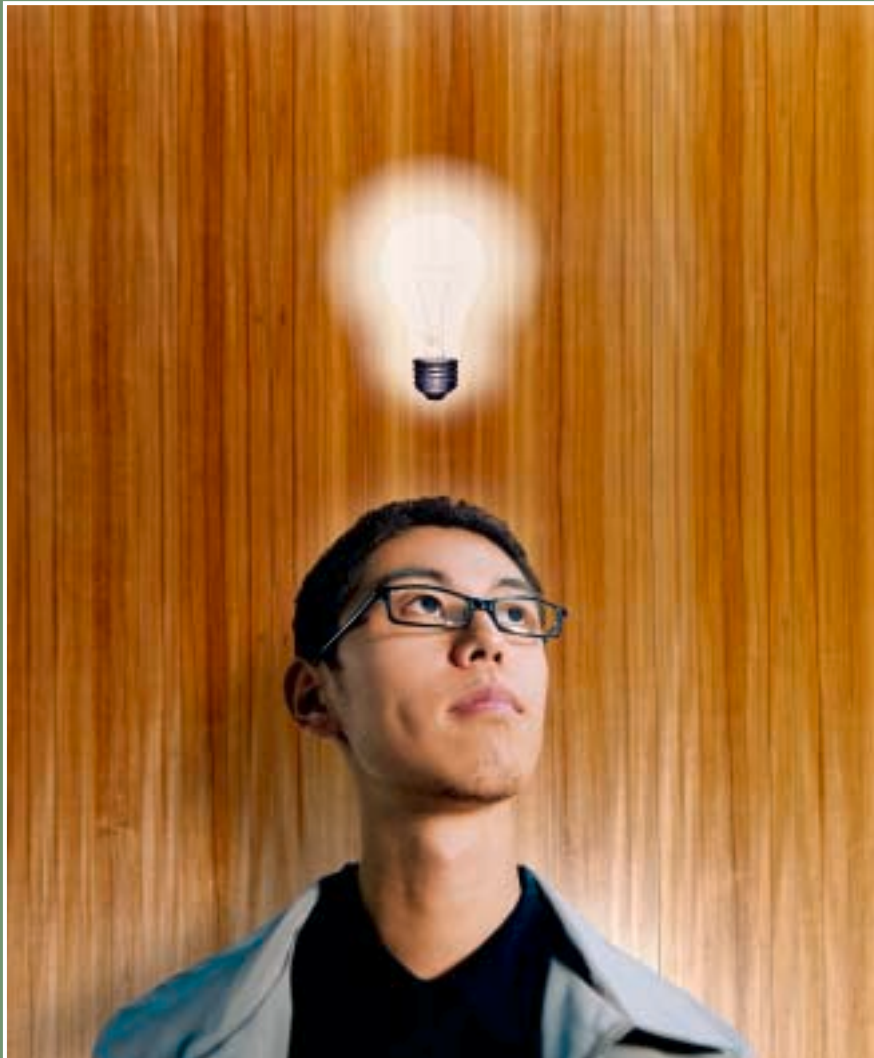
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The innovators



Phone photos SCALE UP

By Junko Yoshida
As the features on feature phones go largely unused and the cell phone industry ponders a back-to-basics strategy, Ramesh Singh is betting his start-up's SoCs can reframe the debate. Singh is a co-founder of Nethra Imaging Inc., which today will launch system-on-chip engines for high-performance processing of 3-megapixel images on camera
CONTINUED ON PAGE 98

IBM claims edge on EDA guard in statistical tools

By Richard Goering

Santa Cruz, Calif. — IBM Corp. is making its most ambitious foray to date into the electronic design automation market with EinsTimer, a commercial spin of the statistical timing tool that the company has been using internally for roughly a year. The suite is available for licensing from IBM's Engineering and Technology Services (ET&S) division, which will offer it along with chip design services.

IBM has been down the commercial EDA road before, with limited success. The company hopes for a better result with EinsTimer, which it calls the first commercially available tool for incremental statistical timing analysis. The tool can be easily integrated into existing design flows and does not require the use of IBM fabrication facilities, though they are available to EinsTimer users, IBM said.

In an era of variability, statistical timing promises to maximize chip performance and yield. Instead of single numbers, it returns probability distributions, sensitivity graphs and yield curves. It can tell a designer how well a design will yield across a frequency range or predict worst-case performance across process variations.

However, there is disagreement over who needs statistical timing and when. And the announcement puts IBM into competition with EDA vendors that have already announced plans to launch statistical timers, including Magma Design Automation and startup Extreme DA Corp., and may set the stage for future competition with Cadence Design Systems and Synopsys.

But IBM is confident EinsTimer will prove compelling. "This is really the industry's first incremental statistical timing analysis capability, including support for both front- and back-end environmental variations," said Dale Hoffman, CTO of IBM Engineering and Technology Services.

CONTINUED ON PAGE 96



Visweswariah: Statistical shift requires open minds.

Passing the baton

Intel's tech group gets new chief as it ponders 45-nm transition

By David Lammers

Austin, Texas — CEO Craig Barrett's handing of the reins to Paul Otellini is not the only managerial transition of note at Intel Corp.

Sunlin Chou, co-general manager of the Technology Manufacturing Group (Hillsboro, Ore.), retired last month, and successor William Holt takes the helm as the TMG's technology development arm grapples with a transition of another sort: the passage from the 65-nanometer process to 45 nm.

Intel is in the middle of making key decisions for its 45-nm process, moving this summer from "pathfinding" mode to final development. Those decisions involve major technology challenges, ranging from the need for improved dielectrics at the gate and in the interconnect—the high-k and low-k issue—to the need for better software, including design automation tools and advanced process control in the fab.

While few doubt that Moore's Law
CONTINUED ON PAGE 14



William Holt



Sunlin Chou

56 All eyes are on the next wave of solid-state imagers—so-called 'vision chips.' They mimic the functions of the human eye, brain in silicon.



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the week in review

Nortel comeback?

Showing signs of emerging from a year of turmoil, Nortel Networks Corp. signed several telecom agreements last week and updated its financials. Since irregularities in reporting emerged last year, Nortel (Toronto) has waged an uphill battle, overhauling management and repeatedly delaying quarterly financial reports. Nortel finally reported its 2004 earnings May 2. Several deals with major telecom providers suggest the troubled company is in the early stages of a comeback.

Inotera ramps 90 nm

Inotera Memories Inc., the joint venture between Infineon Technologies AG and Nanya Technology Corp., is transitioning to 90-nm DRAM manufacturing. Infineon (Munich, Germany), which has already moved 5 percent of its production to 90 nm, said that together with Nanya (Taoyuan, Taiwan), it has qualified the jointly developed 90-nm DRAM technology. Both companies, it said, have qualified 90-nm memories at major customers, including Intel Corp.

Cree drops RF unit

Cree Inc. (Durham, N.C.) will close an unprofitable silicon RF and microwave semiconductor

plant in California to focus on silicon carbide and gallium nitride RF and microwave products. A subsidiary, Cree Microwave Inc., runs the Sunnyvale plant, which makes silicon microwave chips using laterally diffused metal oxide semiconductor (LDMOS) technology. Cree Microwave will accept last-time-buy orders for silicon LDMOS products through this month and close the facility in December. Cree reportedly plans to lay off 80 employees in Sunnyvale.

Estimation tool rolls

Giga Scale Integration Corp. plans to upgrade its InCyte chip estimation tool this week, adding what it calls the first comprehensive IC economic analysis engine. It takes a high-level design specification at the architectural level and provides a complete IC budgetary quotation and final chip cost.

India software boom

Software and service exports in India grossed \$12 billion in 2004-05, up from \$9.2 billion in 2003-04, according to the National Association of Software and Service Companies (Nasscom). With a large labor pool and favorable labor costs, India remains the world's lead-

ing exporter of software services. Similar growth is predicted for 2005-06, Nasscom said.

TSMC, UMC gear up

Two top foundries, Taiwan Semiconductor Manufacturing Co. Ltd. and United Microelectronics Corp., have lengthened lead times for their products as they boost manufacturing capacity utilization rates due to increased orders. Delivery times last quarter were six to seven weeks. Now, after some utilization realignments, lead times have gone from eight to nine weeks. Some 6-inch wafer fabs now have 10-week lead times.

Lightning-fast laser

An 850-nm wavelength AlGaAs/GaAs vertical-cavity surface-emitting laser from Matsushita Electric Co. (Osaka, Japan) claims a 12.5-Gbit/sec data transmission speed at an operating current of 8 milliamperes. The laser will target plastic fiber communication and spatial light transmission.

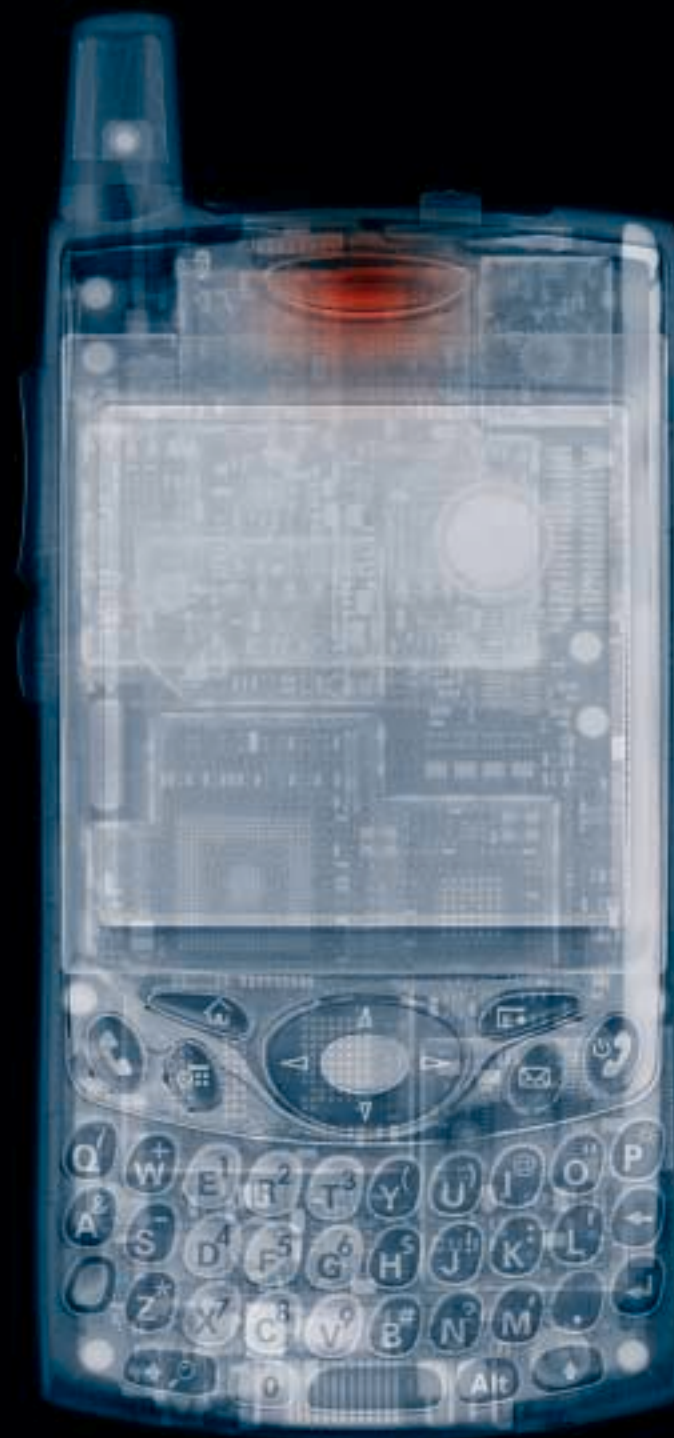
Correction



Stephen Lee

An article on page 76 of today's edition by Stephen Lee, an applications engineer at Analog Devices Inc., includes the wrong author photo. The correct photo appears here.

When an electronics company
needs to integrate
three devices into one,
and make it all fit in your hand,
we hear the call.



A phone that thinks it's a PDA. A PDA that lets you surf the web without wires. Smart idea. From smartphones to MP3 players to digital cameras, electronics companies face tremendous challenges developing new products. Consumers expect devices to do more yet run longer on battery power. Entire systems need to fit in your pocket. And products with tens of millions of transistors can't run too hot to handle. How do our customers overcome the odds and create the advanced ICs, packages, and board-level systems that hide inside these small wonders? They do it by using electronic design software, methodologies, and services from Cadence to achieve breakthrough results at almost every turn. For more information, visit www.cadence.com/heartheall.

As budget deficits and war costs cut into federal R&D spending, it's time to raise the alarm in Washington

Keep our IT research on track

Government funding for basic research in information technology appears to be plummeting, triggering fears that the United States will lose, over the long term, its advanced-technology lead. IT has become a cornerstone of the economy and is pivotal to just about every scientific and engineering enterprise. And of course, national pride figures in the growing concern for the future of U.S. technology.

Budget proposals for 2006 from the various government agencies that fund research in IT show a general downward trend. Reduced funding may simply be the result of current fiscal stresses brought on by high budget deficits and the war in Iraq. Or it may indicate a changing set of priorities in the administration.

How serious is the shortfall?

In a guest editorial in a recent issue of the American Association for the Advancement of Science's flagship journal, *Science*, David Patterson, president of the Association for Computing Machinery, and Edward Lazowska, a computer scientist at the University of Washington, maintain that reduced funding is only part of a larger worrisome pattern. The Defense Advanced Research Projects Agency's review process has become much more difficult for academics to meet, they note, and the projects Darpa approves are directed far more at top-secret military efforts with immediate goals, taking away funding for fundamental research with long-term benefits.

Other critics of the administration say that immigration restrictions stemming from the war on terror make it difficult for talented foreign students and researchers to study and work at U.S. universities. It would be a shame if the unique qualities that make the United States

a technology leader—generous funding, a heterogeneous culture, the open flow of ideas—are in decline.

It is always difficult to predict the impact of short-term perturbations in funding and science policy. But raising the alarm seems to be a healthy exercise for scientists and engineers, who care deeply about the possible consequences of government policy.

Yet it is also important to realize that concern over funding is not just a U.S. phenomenon. Sharp cuts in funding for research in France over the past three years finally sparked a nationwide revolt by academics. A petition revealed that 80 percent of the French public was in favor of higher funding and, in March, about half of France's laboratory research directors met in Paris to offer their resignations. The result: an about-face by the French government, which restored the large number of research positions it had cut and increased the science budget by 10 percent.

I am sure the American public is equally concerned about the future of technology here. Darpa itself was a response to the alarm generated by Sputnik in the 1950s. Widespread concern in the 1980s over a perceived Japanese lead in computer technology led to



increased IT funding. Indeed, that effort has been credited with the rise in U.S. productivity of the 1990s.

There is solid reason to remain optimistic about the quality of IT research in the United States. But once in a while, a dose of alarm may be a bracing restorative to keep the program on track.

By Chappell Brown (cbrown@cmp.com), technology editor for EE Times

Let Moe, not formats, knock heads together

Call me a Luddite, but at 47 I have collected my fair share of media libraries and have little enthusiasm for whatever Hollywood's next big format might be.

That next format is bits running over a network—any network. Music will be bits, movies will be bits, TV will be bits. But neither I nor most of the technologists whom I admire seem to have the power to see into the convoluted future of business and regulatory practices that may prevent this shift to bits from happening in my lifetime.

By Rick Merritt, editor at-large for EE Times

Instead we are likely to see another couple of generations of superdense, enhanced and extra-interactive disks of various sizes—and maybe a few flavors of fingernail-size flash cards that can fit into any device you own, as long as you get a special caddy from Radio Shack. What a mess! As content owners and carriers scramble to protect their multibillion-dollar revenue streams, they are likely to give my kids the opportunity to amass a few media libraries of their own, just as I bought 45's, LPs, eight-tacks, cassettes, VHS tapes and DVDs. Ah, capitalism!

On really bad days, I just wish for a little light-hearted communism, perhaps in the form of Moe Howard of

the Three Stooges. Someone who would knock some heads together without really hurting anyone.

"Now listen youse guys," my fantasy Moe would say to Carrier Curly, Studio Shemp and Larry the Lobbyist. "Here's what were gonna do ... it's gonna be bits, see ... over the wire, see ... so get that through yer thick heads, ya numskulls!" (Slap, slap. Thunk, thunk.)

After the reign of Moe, I'd get an MP3 player for jogging. I'd finally buy a new TV and stereo—ones that connect to the Web—and a telematics gizmo for my car. I'd sign up for a couple of subscription programs after checking out the deals available. I'd be in bit heaven.

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Tool for capturing comms protocols debuts

By Richard Goering

Santa Cruz, Calif. — After leading the architectural-validation effort for Intel Corp.'s P6 processor core, Reed Christensen decided there must be a better way. The result was Bellum Software, a startup that's developed a protocol capture tool that handles data in a graphical format. The tool will roll out at the Design Automation Conference next week.

In addition to the Protocollum tool, which allows communications systems engineers to capture, edit and test a protocol architectural specification, Bellum is bringing a familiar name back to the EDA industry. Bob Hunter, former president of HDL simulation pioneer Model Technology, serves as the Hillsboro, Ore., company's vice president of marketing and sales.

Christensen, the president of Bellum Software, is basing his new company's tool on observations gleaned from 12 years at Intel. "The issues we had at Intel about how you write clear specifications for validation, and how they get communicated, are still around and we haven't made a lot of progress," he said. "My impression is that most teams are using homegrown tools or are using various languages to write their own models. There doesn't appear to be much of an effort in trying to do that in a graphical or visual way."

After leaving Intel in 2001, Christensen

said, he came across a paper from an IBM Corp. research group in Zurich, Switzerland, that showed there might be a better way to model communications protocols.

Christensen had been concerned about this issue, he said, because of a realization that most bugs occur in the interfaces between functional units. He originally thought that message sequence charts might be a good way to model communication between units, but these are primarily static diagrams drawn in PowerPoint or Word. "What I wanted was an executable running system, where you could change diagrams on the fly," Christensen said. "What I got out of the [IBM] research paper was an approach to doing that. Basically, they had a rule-based system that allows you to create and plot events in a graphical environment."

He developed Protocollum on his own, and only recently began talking to some marketing people and developing a Web site at www.bellum.biz. Christensen then approached Hunter as an adviser, and so impressed Hunter that he set aside his seven years as a "gentleman farmer" to join the self-funded startup.

"I'd been doing this and that, but nothing really in the professional world," Hunter said. "This is just a very, very interesting tool that might offer a lot of value. I found it really intriguing. And I think I have enough background with enough contacts to make a little headway and get some exposure with engineering groups in the U.S."



Christensen: Protocollum generates graphical model.

Bellum's overall mission, said Christensen, is "putting good tools in the hands of computer architects." Protocols are a good place to start, he said, because they're so pervasively used and because there's been little progress in how they're developed.

Today, said Christensen, most people model protocols by designing state machines in languages like C, SystemC, VHDL or Verilog. Protocollum allows the same thing, he said, although it takes place in a graphical environment. "If you're writing lines and lines of code, you can't see or visualize what the flow of the system is," he said.

Protocollum allows designers to set up much of their system through point-and-click operations. State machines do need to be specified in code, which is done

through Tcl scripting. But even that, said Christensen, becomes input for a graphical model.

Once an architecture is captured, users have an executable specification. Users can set up a "test sheet" that establishes various message-passing scenarios. By observing states, they can see if the system is behaving as they expected.

Christensen said that early adopters have mostly been hardware engineers, although the tool could be used prior to hardware/software partitioning. There is, however, no direct connection to downstream implementation, since Protocollum does not generate SystemC or HDL code.

At a time when many EDA tools cost upward of \$100,000, Protocollum has what may be a refreshing price tag—\$995. Some of the distribution will be through the company's Web site. "We're starting out small," Hunter said. "We're not going to overmarket this thing."

Christensen gave Protocollum a road test himself on the 802.11 specification, finding a bug in that 1999 specification in the process. But the tool isn't just about large, well-known communications protocols, he said. "Chip design has plenty of communications in it. We just haven't been too formal in how we specify that and pass it to other designers."

Organic molecule switches like a transistor

By R. Colin Johnson

Portland, Ore. — Researchers at the University of Alberta have successfully demonstrated a single-molecule switch and transistor.

"There is no longer a question of whether a single molecule can be used as a switch; we have shown that it can be done," professor Robert Wolkow said. "Also, we have demonstrated how you can get two electrodes to act like the three electrodes normally associated with a transistor. In particular, we have shown that a chargeable atom can act as a gate using the same electrode that is also acting as the source."

But there's a caveat: "We don't yet have any kind of realistic temporal control" of the switch," Wolkow said. "Right now, it takes minutes to turn it on and off."

Working with postdoctoral fellows Paul Piva and Stanislav Dogel, as well as graduate student Janik Zikovskiy, Wolkow's team placed a single organic molecule on a silicon substrate so that the molecule acted as the transistor channel, with the substrate acting as a back gate for switching. The work was performed in cooperation with staff scientists and their postdoctoral assistants at the National Institute for Nanotechnology, which is a part of the National Research Council of Canada, as well as with professor Werner Hofer of the Surface Science Research Centre at Britain's University of Liverpool.

Other research groups have been working to achieve uncontested demonstrations of single-molecule transistors, but their results have not been rock solid, according to Wolkow. The problem has been trying to guarantee that the electrodes connecting to the

molecule are in fact switching it. Molecules are so small that it is difficult to attach electrodes to them in a verifiable manner, Wolkow said.

That's where the Alberta team's two-electrode approach comes into play. Ordinarily, Wolkow said, "electrodes attached to a single molecule are just too small to get a gate near enough to operate efficiently, which limits how big a field you can drive onto the molecule. What we have is a trick to make two electrodes act like three, because our single atom is at a different potential—approximately 1 volt—than the rest of the silicon surface, even though it is charged with just a single electron and is just angstroms away from the other atoms around it."

Wolkow's group has been working with many organic molecules, learning how to bond them to silicon substrates and get them to line up into rows. But the current demonstration is the first to inject electrons into the molecule.

"We use an ordinary silicon substrate that is hydrogen-terminated," Wolkow said. "By removing a single hydrogen atom, we create a dangling bond, to which we attach a single

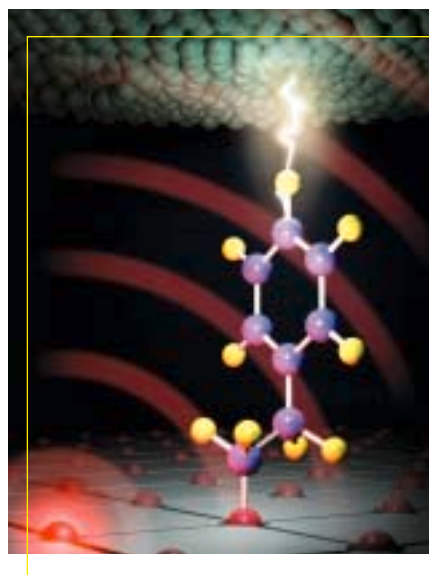
monomer molecule called styrene." The styrene molecule is attached to the surface with a carbon-to-silicon bond.

"The trick is that as the styrene molecule becomes bonded to the surface, it attracts another hydrogen atom from the silicon surface, thereby creating a second dangling bond, which is at a different potential than all the other silicon atoms on the surface. Thus, by changing the potential on the whole surface, we can cause that one silicon atom to be charged or not with a single electron."

The other contact to the molecule—the drain—is the tip of a scanning tunneling microscope (STM).

"We demonstrated we can control current through the styrene molecule in the same way that a field-effect transistor works, with the substrate acting as the source and the STM tip acting as the drain," Wolkow said.

For the future, Wolkow wants to form a line of organic molecules, with the first one attached to on-chip electrodes that will act as the source and drain.



Sketch shows the silicon substrate (source), red dangling bond (gate), tunnel electrode (drain) and molecule (channel).

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Chip interconnect draws designers, too

Scaling issues at 65 nm likely to expand the crowd at ITC

By Ron Wilson

Fremont, Calif. — The eighth annual International Interconnect Technology Conference opens today to a growing—and unfamiliar—level of attention. Traditionally a highly specialized forum for the process engineers who create interconnect stacks on ICs, the event has already begun to reach beyond its normal audience, attracting chip designers as well.

“Interconnect scaling is not like transistor scaling,” said Mark Bohr, senior Intel Fellow. “As you make transistors smaller, they get faster. That is no longer true of interconnect. As you reduce the width of interconnect segments, you also have to reduce the thickness, and so the resistivity doesn’t go down.”

This fact was a significant factor in Intel’s shift from ever-faster uniprocessor chips to multicore chips, Bohr said.

John Martin, vice president of strategic alliances and partners at Chartered Semiconductor Manufacturing Ltd., looked at the issues his organization sees in the transition from 90-nanometer to 65-nm interconnect and divided them into three categories: patterning, dimensional control and chip-to-package interactions. Of those, perhaps the most significant is patterning.

To deliver the density promised by those smaller transistors, the first few metal layers in a 65-nm process must allow for very fine metal pitches. At 90 nm, for the first time, the pitch on Metal-1 became so tight that optical proximity correction was necessary to correctly render the patterns on the Metal-1 masks.

At 65 nm, OPC may be necessary on several more metal layers. While vendors are very hesitant to reveal exactly which layers require OPC, Intel’s Bohr did say that in Intel’s 65-nm process, Metal-1 through Metal-3 all had to be exposed on 193-nm steppers. Presumably, they all require OPC as well.

“I can say that we have put considerable effort into OPC—making sure that the features we are creating are the geometries the designers intended,” Martin said. “This is especially true in the 1x layers—those with the finest metal pitch.”

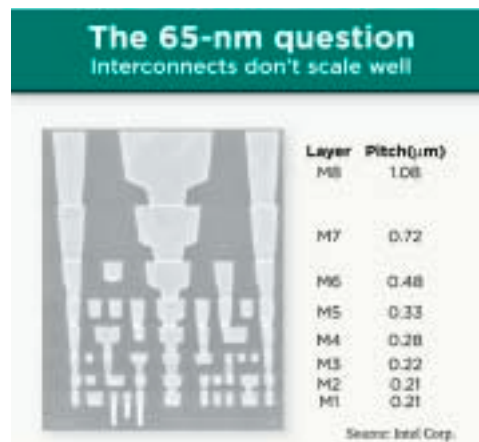
Layers that require OPC also require very intimate interaction among process engineers, mask makers and the chip physical design team, to make sure that the designers’ intent is being honored in the metal. When OPC use was limited to Metal-1, this only meant that cell designers had to work closely with the fab—which is nothing new. But as the requirement moves up the interconnect stack, that fellowship may have to be extended even to designers who are simply placing and routing standard-cell designs. It is easy for existing place and route tools to create patterns incompatible with OPC.

“Right now we are on the threshold of

the point where layers created by the design team will require inspection for OPC compatibility,” Martin said. “At some point soon we will have to work together closely with design teams on the ability to create mask patterns that can render their intent.”

That close relationship already has to exist for another area of checks—dimensional control—and it will only become more intimate at 65 nm.

Even if the right patterns are created in the photoresist, there are several problems to be solved before the right shapes actually exist in the metal and dielectric materials. Chemical-mechanical polish-



ing is one of the hurdles. The interaction between the rotating polishing disk, the polishing material and the surface of the wafer is quite complex and—unfortunately for designers—highly pattern-dependent. The orientation and shape of lines and especially their spatial distribution will determine how much metal is removed during polishing.

Other variations arise from the lithography process, where variations in focus can cause width variations; in deposition, where the thickness of films can vary; and in etching, which can introduce further variations while translating an opening in a resist layer into a trench in the underlying material. All of these variations accumulate and translate into variations in the resistance and capacitance of interconnect segments.

“Modeling interconnect delay is a serious issue,” Bohr said. “Now we are at the point where we simply need more complex models to reflect the expected shape of the interconnect as you go through various sizes of segments and various vias. Simple lumped models aren’t going to cut it.”

But starting perhaps just beyond 65 nm, the problem will get worse. Bohr warned that the variations in interconnect geometry were approaching the importance of the widely discussed variations in transistor parameters. “Already it’s not feasible to do worst-case design. You have to account for transistor variations with some sort of statistical design technique, or you leave too much on the table and produce an uncompetitive design,” Bohr said. “That is gradually

becoming true for interconnect as well. But we aren’t there yet at 65 nm.”

One reason we aren’t there yet is heroic effort on the part of process integration engineers. Intel, for example, has attacked problems in via formation so successfully that its design rules do not require redundant vias in signal paths. “There are things you can do, such as filling the vias with copper and doing barriers correctly, that help with via formation,” Bohr said.

Chartered, with its process development partners IBM, Infineon and Samsung, is fighting a similar battle on dimensional variations. “A big factor is the automated precision manufacturing process control system Chartered has licensed from AMD,” Martin said. “One of the focuses of APM is the polishing process and controlling the variability it can create. Our data so far indicates that it will be effective in our foundry environment as well as in AMD’s mass-production environment.”

“But another important component,” Martin added, “will be working with design teams to control the pattern density across the die so that the polisher is working on a relatively uniform surface.”

Looking beyond 65 nm, the path is less clear. As metal geometries shrink, it is critical to reduce the dielectric constant of the insulating material. But Bohr said so far there have been only minor improvements in k. “We changed to a lower-k etch-stop layer, which helped the k-effective of the whole stack,” he said. “But the best way we have of reducing capacitance between lines right now is to add metal layers to reduce congestion. We can’t keep doing that forever.”

“I expect that, by 45 nm, we will have selected a suitable new dielectric material,” Martin said. “There simply wasn’t one available in time for 65 nm that had appropriate mechanical and process-integration characteristics.”

The candidates today remain problematic. “Copper in thin films—such as in lower metal layers—is very weak,” observed David Wang, president and CEO of noncontact polishing vendor ACM Research Inc. “We can use mechanical polishing today because the thin metal ribbons get mechanical support from the dielectric material in which they are lying. But copper has a Young’s modulus of about 40. The new low-k materials are around 3. They aren’t going to support the copper, and it is going to be deformed beyond its elastic limit if you try to mechanically polish it and you aren’t very careful.”

The picture at 65 nm remains guardedly optimistic, with almost no materials changes—none at all in Chartered’s case—from 90 nm. But 65-nm designs will still require more effective process controls and closer work with design teams. At 45 nm, there are still many answers missing. But no one will be able to take interconnect for granted.

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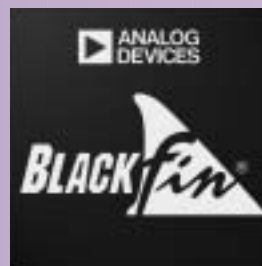
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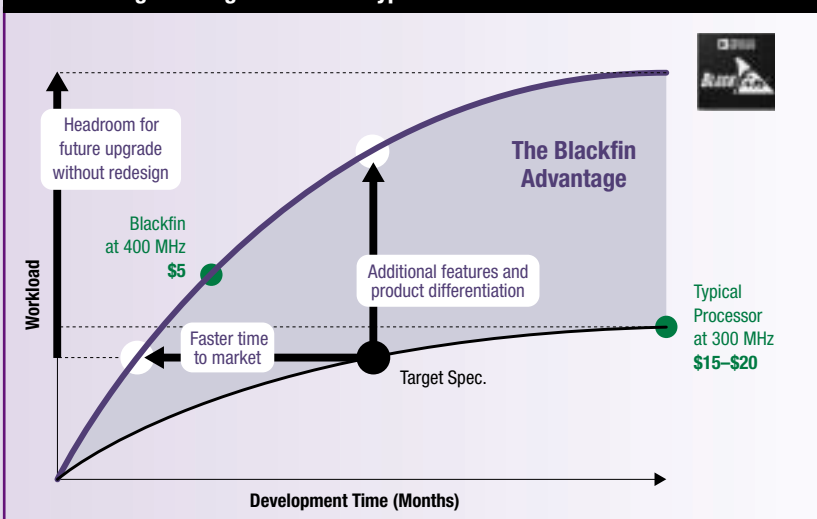
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Platform strategy fuels Wind River rebound

By David Lammers

Orlando, Fla. — Ken Klein, who took over as chief executive officer of Wind River Systems Inc. 18 months ago, kicked off the company's users' conference here last month in slightly contrarian fashion. The company that rode the VxWorks operating system for its first two decades is now "OS-agnostic," Klein said, declaring that "the OS is not our core business."

Wind River has gone well beyond a U-turn on Linux, which earlier management publicly opposed. This year, its engineers have taken the lead in adapting the open-source Eclipse platform—which started within IBM as an IT-centric user interface—to the needs of embedded-software developers.

Rather than using VxWorks as its leading punch, Wind River has adopted a platform strategy—packaging the appropriate OS, middleware and run-time tools—tailored to major industry segments, said chief marketing officer John Bruggeman. As part of that strategy, the Alameda, Calif., company has courted smaller software vendors as partners—companies that got mostly lip service from Wind River until recently.

Steering a tanker

For example, Wind River and Express Logic Corp. have started cooperating, going on joint sales calls to pitch Express Logic's compact ThreadX operating system to customers that need a small-foot-

Shifting Wind

Refocus has intensified during the past two years

1981	Jerry Fiddler and David Wilner found Wind River Systems Inc.
1987	VxWorks operating system launched
1993	IPO on the Nasdaq exchange with the symbol WIND
1994	Ron Abelman named CEO
1995	Tornado integrated development environment launched
1998	Acquisitions help grow head count from 700 to more than 1,700
1999	Former Applied Materials executive Tom St. Dennis named CEO; he opposes Linux; full Java compatibility for an RTOS certified
2000	Integrated Systems Inc. and its pSOS operating system acquired for more than \$900 million
2001	Revenue peaks at \$438 million for the fiscal year; Berkeley Software Design Inc. acquired
2003	Ken Klein named CEO; management shakeup; first tool and services support for Linux offered
2004	Eclipse-based Workbench rolls, supporting VxWorks, Linux; Wind River partners with Red Hat, delivers Linux platform for net gear
2005	Becomes strategic developer of Eclipse Foundation

Source: EE Times

print, royalty-free OS in combination with support tools and service from Wind River.

Such partnerships "would have been unthinkable" under the previous Wind River management, said John Carbone, vice president of marketing at Express Logic (San Diego). "The new team took a tanker that was headed for the rocks and steered



'The OS is not our core business,' says CEO Klein.

it back into the middle of the river. That's hard to do," he said.

Beset by an industry downturn and its own mistakes, Wind River watched as its annual revenues dropped by more than half after peaking at \$438 million in 2001. About 1,000 people—nearly half the work force—were laid off during the downturn, said chief technology officer

Tomas Evensen, who joined Wind River as part of its 2000 acquisition of Integrated Systems Inc.

"The layoffs were very hard on morale. The uptick in engineering morale actually started earlier [than the changes in management]," Evensen said. "We got rid of the separate business units and created one engineering unit under Scot [Morrison, vice president of engineering]. From an engineering point of view, that was the start of the turnaround."

Starting three years ago, Wind River

CONTINUED ON PAGE 29

Web tool readied for data converter IC match

By Stephan Ohr

San Francisco — National Semiconductor Corp. sees the introduction of its Signal Path Designer tool set as another stepping-stone into a burgeoning market for data converter ICs.

The online design aid—part of National's Webench circuit analysis suite—will let designers simulate the cumulative behavior of the company's data converters with their front-end amplifiers and signal conditioners. Combined with new families of high-speed data converters, the tool set will bring increased visibility to its A/D and D/A converter products, National said.

"We're jumping into the data conversion market with both feet," said Phil Gibson, National's vice president and director of corporate marketing.

Currently, some 6 percent of National's \$2 billion business is in data converters, which makes it No. 4 in a 2004 market estimated between \$2.4 billion and \$2.6 billion. Analysts agree that Analog Devices Inc. is the most influential player in this sector, with more than 40 percent of the market. But there is some dispute over the relative positions of the

next two companies, Texas Instruments Inc. and Maxim Integrated Products.

National's data converter strategy has two elements, Gibson explained. One consists of releasing high-speed data converter families in which each part varies in terms of resolution but is linked to the others by conversion speed, multiplexer configurations and package types. The general-purpose successive-approximation register (SAR) types, for example, offer sample rates to 1 MHz and pin compatibility among 8-, 10 and 12-bit versions with the same mux.

High-speed parts like the ADC08D1000 dual A/D with a 1-Gsample/second rate—for receiver I-and-Q extraction—will offer a similar affinity with new additions to its product line.

The second element of the strategy embodies what product line director Antonio Visconti has called "a big stick" approach: "You don't want to fight the big guy head-on," Visconti told *EE Times* in April. "But you can

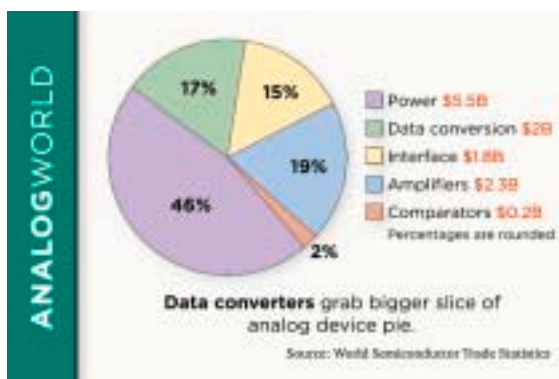
sneak up behind him with a stick."

Easy-to-use design evaluators, like the company's Webench online tools, become part of the big-stick approach, Gibson said. The Signal Path Designer

ter topology or transfer function and find the semiconductor elements that best execute that function.

Using an on-screen entry form for desired specifications (and radio click buttons for filter topologies), the tool will identify an appropriate data converter, construct an anti-aliasing filter and provide a waveform output of performance, complete with tolerances and temperature coefficients.

Webench tools for power supply and amplifier design attract close to 8,000 engineering visitors a month, Gibson said, and collectively they represent some 20,000 new designs—90 percent of them constructed in a virtual mode. The general-purpose 8- to 12-bit SAR converters will be the first devices simulated with Signal Path Designer. Later iterations of the tool will add not only the ability to simulate the performance of high-speed converters, but also the ability to visualize this performance in the frequency and time domains.



tool helps designers visualize the behavior of signal-conditioning systems with a number of amplifiers and data converters.

The tool set allows designers to select a data converter topology and match an appropriate signal-conditioning front end to it, Gibson explained. Alternatively, designers can start with a particular fil-

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Intel eyes 45 nm

FROM PAGE 1

scaling will continue in terms of raw transistor density improvements, skeptics question whether the smaller transistors will show proportionate performance gains. And beginning at the 90-nm node, power consumption has proved contentious, leading Intel to downscale its emphasis on raw megahertz and move to dual-core architectures running at slightly slower speeds.

Chou, who retired at 58 after 34 years at Intel, said that performance gains have never come easily. At the beginning of each node, engineers wring their hands, doubting that performance goals can be met, only to come up with process innovations that save the day. Going forward, Chou said, the fact that smaller transistors drive smaller loads will help in the struggle to gain performance. Innovation will supply the rest.

"Strained silicon is an excellent example of a new technique that improves mobility," he said. "That was not accomplished by pushing the classical, evolutionary techniques. The high-k gate dielectric is another one of those kinds of innovations that give us performance improvements."

Chou ran the unit's research and technology development arm—the "T" of the 34,000-person TMG—since 1998, managing "synchronized development," or the simultaneous development of the device and process; packaging and test; and design tools and design collateral, such as the transistor models. Senior vice president Bill Baker continues to manage manufacturing operations. Since 1986, beginning with the 1.5-micron generation, Chou led logic technology development at Intel.

What about high-k?

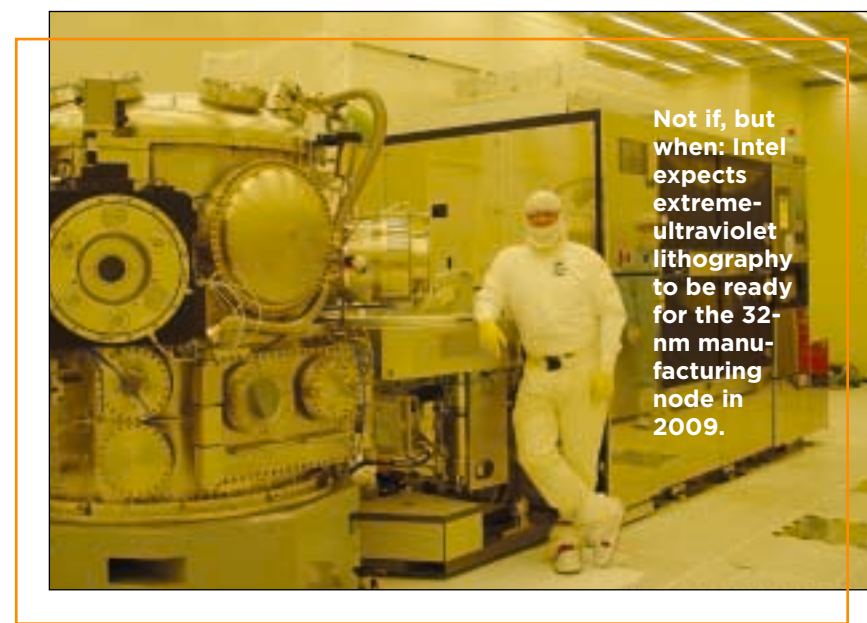
Intel announced two years ago, at a conference in Japan, that it had identified a combination of a high-k dielectric and a metal as the gate electrode. The combination was described as a candidate with possibilities—a gate stack that had the potential to supplant the combination of silicon dioxide as the gate oxide and polysilicon as the gate electrode. At the time, Intel said that if the high-k option was not mature enough for introduction at the 45-nm node, then the company would consider a more drastic move, away from planar transistors and toward a FinFET or trigate-type structure using silicon dioxide.

That was 2003. This year, technology managers at both Taiwan Semiconductor Manufacturing Co. Ltd. and Texas Instruments Inc. publicly have expressed doubts that a high-k dielectric can be reliably introduced at the 45-nm node, given the continuing challenges with threshold-voltage stability. Many now believe the industry will try to use a nitrided form of silicon dioxide again at the 45-nm node, despite the fact that the thickness of the oxide layer cannot be scaled beyond the approximately 1.2 nm (12 angstroms) used for both the 90-nm and 65-nm nodes.

For Intel and other technology leaders,

the time for making a go-or-no-go decision on high-k is drawing nigh, since managers must freeze their materials set for the 45-nm node this summer.

Chou said the 2003 announcement (which did not identify either the high-k or the metal gate material) signified that "we had convinced ourselves there was a way to make high-k work, but that we would need more development. We saw it as an option for the 45-nm process. That statement is absolutely still true today, despite various speculations about it looking better or not."



Not if, but when: Intel expects extreme-ultraviolet lithography to be ready for the 32-nm manufacturing node in 2009.

Intel enters a "quiet period" once it decides on the materials and equipment options that will be introduced at a new technology node. Then, once the process gets close to full production, Intel opens the kimono somewhat to reveal some information about those process innovations.

Asked if Intel was considering using a metal gate electrode with the nitrided oxide now in use, Holt said, "We don't want to go to that level of detail" but added, "If we were to go in that direction, we would not get the advantage of reduced oxide leakage, which is the advantage of a new dielectric."

Combining a nitrided silicon dioxide with a metal gate might reduce polysilicon depletion, which could provide some gain in performance compared with the traditional SiO₂/poly stack. "Poly depletion would improve and, yes, that would provide some gain on the performance side, but not substantially on the leakage side," Holt said. "There are lots of different approaches, and we are not at the stage of saying what we are doing."

In Chou's opinion, "High-k has a lot of potential to help us in the future to continue to address fundamental scaling issues that in the past were viewed as hard limits."

Aside from the high-k issue, Chou said Intel's circuit designers and process technologists are working more closely together to reduce power consumption. At one point, the industry became convinced that supply voltages could not be scaled below 1 V. Since then, technologists have become more confident that V_{dd} can be reduced to 0.8 V or less. Also, circuit

designers have come up with techniques to save power, including putting circuits to sleep while they are unneeded.

"We are still scratching the surface in terms of turning off inactive circuit blocks," Chou said. "Can we scale below a volt? The answer is yes. Beyond that, there are enormous savings in the circuit design area."

Intel's technologists are working on other areas that are less visible. Holt said the group has long worked on fundamental process modeling, with internal BSIM models and transistor extraction tools

developed as part of the process of bringing up any new technology node.

Advanced process control, Holt said, is an area "where we have significant capability. We have begun to expose some of the automation [publicly]. We are beginning to write some papers."

Intel for some time has had the ability to adjust its downstream process steps based on feedback from a previous step. It can "feed forward" adjustments to the etch process and use them to improve critical-dimension control.

"We look at where we get the maximum return" from advanced process control, Holt said. "We are not deploying it just for the sake of deploying, but where we get the most return. We have process feedback, where we look at previous steps and apply it to subsequent steps."

As part of Intel's "copy exactly" method of transferring a technology into manufacturing, the technology manufacturing group oversees the entire automation system, including all of the process control modules. Design-for-manufacturing (DFM) is another weapon in the broader effort to obtain good yields. The group continues to refine yield analysis tools, which bring in large volumes of information to tools that analyze subtle differences in the performance of manufacturing equipment, or analyze how yields differ depending on the position of the die on the wafer.

"We begin yield improvements when we start the process development," Holt said. "Yield improvement is not something we bolt on at the end. We have to design in the margins, understand what the

process is capable of and then feed that back into the design process. It's called DFM, but we have to start by knowing what the manufacturing is capable of and then feed that back into the design process."

This ability to share information among the process technologists, the chip design teams and the manufacturing engineers makes it possible for Intel to "integrate these activities and get something out of it that is greater than the sum of the parts," Chou said.

"There are increasing interactions between design and process technology," he said. "For chemical-mechanical polishing, to achieve good uniformity, that is dependent on the layout geometry of a single layer. We have to put dummy patterns in just the right places. It is a very sophisticated interaction that requires sophisticated tools to model the results before we try it in silicon."

Holt cited statistical timing as an increasingly important technology. One area that is in the early stages of widespread application involves probabilistic simulation tools that look at statistical variations down a path. Those variations can be applied to a timing tool.

"Variability clearly is something we are going to have to live with," he said.

Asked if Intel has taken possession of an immersion lithography tool, Chou declined to detail the road map for immersion, which many vendors expect to come into widespread use for the 45-nm node.

"We absolutely will evaluate immersion, and if it works we will certainly consider it," said Chou. At the moment, he said, "the industry as a whole does not have that definitive information. It will take several months, by my reckoning, before that definitive information is available."

Intel's lithography road map calls for extreme-ultraviolet (EUV) lithography to be ready for the 32-nm node, or in the 2009 time frame. And Intel managers have emphasized that EUV-based scanners must meet productivity and cost targets for high-volume manufacturing.

"If there was a make-or-buy year [for EUV], that came some time ago," he said. "EUV has proven to be technically feasible, and now the emphasis has changed from the pure technical challenges to the commercial challenges. We are making tremendous progress in areas such as the source power [for generation of the EUV radiation]. There are so many different suppliers of the EUV source, with so many different approaches, that it's just something that is going to work its way out."

Attention has now turned to getting defect-free mask blanks, he said, "and in that area we have seen a fortyfold improvement in defects over the past 18 months. We are within a factor of 10 of our target, and if you extrapolate the rate of progress, we will solve that challenge as well. So we are increasingly optimistic about EUV."

Chou pointed to "the increasing amounts of money that are being invested in EUV development by all of the suppliers, in all parts of the system," as a sign of "the industrywide confidence" in EUV. "Now it's a matter of not if, but when," Chou said.

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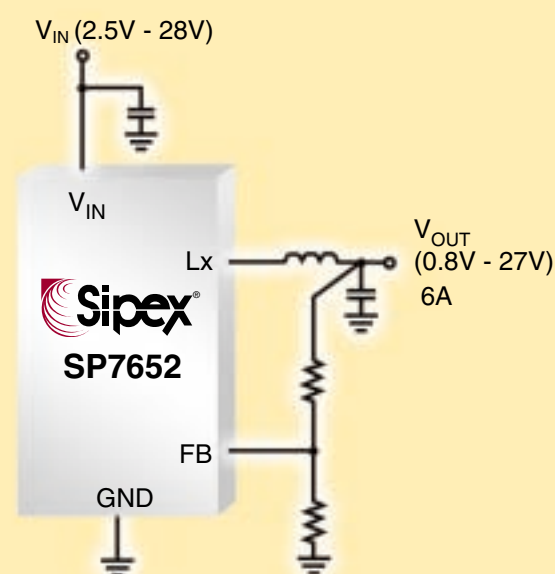
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Nanotech conference plots future of electronics

By R. Colin Johnson

Portland, Ore. — Presenters at the First International Nanotechnology Conference on Communication and Cooperation last week identified the key issues facing nanotechnology.

"The engineers of future nanoscale devices will have to acquire many different skills that they do not have today, just as they had to do when we made the transition from discrete components to integrated circuits in the past," said Intel Corp. research fellow Paola Gargini.

The San Francisco conference, which hosted more than 36 presenters from nearly a dozen countries, kicked off with overviews of the state of nanotechnology in the United States, Europe and Japan. A dozen presentations zeroed in on the key issues and challenges facing future EEs designing nanoscale devices.

Franz Kreupl, nanoelectronics project manager with Infineon Technologies AG's corporate research labs, described the key issues that remain to be solved in manufacturing chips using carbon nanotubes.

Nanotubes have "huge electron mobil-

ity, mechanical strength and chemical inertness," he said. "Their phase space, because of their nearly one-dimensional aspect ratio, enables almost ballistic electron transport, reduced scattering and an almost complete absence of dangling bonds, making the use of high-k dielectrics simple and easy."

Kreupl speculated that the remaining problems facing the integration of nanoscale devices with traditional silicon processing techniques will require a multidisciplinary approach that combines traditional EE skills with those from materials scientists, chemistry and biology.

University of Tokyo professor Toshiro Hiramoto claimed that combining nanoscale processing steps with traditional silicon devices would yield a new regime of nanodevices that would "enhance mobility with ultrathin transistor channels and enable sub-band engineering with multi-bit operation in silicon nanocrystal memories and single-electron transistors."

Other researchers concentrated on nanowires, organic large-area solar cells, molecular electronics, spintronics, bioanalytic systems and nanotechnology in medicine.

On the last day of the conference, speakers looked at the biological and societal implications of nanotechnology, including the use of organic materials in the fabrication of everything from large-area electronics to artificial organs. Also discussed were the ethical issues facing the safe deployment of processing methodologies and

end-user applications in nanotechnology that hold the potential to shift the worldwide economic balance.

Presenters speculated that chemistry, especially nanoscale catalysts, would be the first technological area to be revolutionized by nanotechnology, followed by semiconductors that employ nanotechnology to indefinitely extend Moore's Law, with a sprinkling of medical break-

throughs along the way.

"Nanotechnology in medicine could profoundly improve the quality of life worldwide, with one of the first breakthroughs likely to be the creation of artificial organs," said Mihail Roco, a key architect of the National Nanotechnology Initiative and chairman of the U.S. National Science and Technology Council's subcommittee on Nanoscale Science, Engineering and Technology. Roco is also a senior adviser in nanotechnology at the National Science Foundation.

The conference was co-organized by Intel Corp., a leading nanotechnology research supporter. Co-sponsors from the United States, Europe and Japan included the National Science Foundation, Sematech, Lux Research, Philips Research Laboratories, Hitachi and the National Nanotechnology Initiative.

Representatives from governmental and industrial organizations in Spain, Japan, Germany, Belgium, Sweden and the United States were among those who provided updates on nanotechnology developments.



Hiramoto advocates combined processing.

Wireless sensor nets made easier

By Patrick Mannion

Manhasset, N.Y. — Moving to speed the design of wireless sensor networks for industrial automation, Sensicast Systems Inc. will introduce a modular platform this week that offers multiple radio and mesh-networking protocol options. In little more than a week, Sensicast said, designers can have a fully certified wireless sensor based on standard IEEE 802.15.4 radios, with either a ZigBee stack or the company's SensiNet protocol for more challenging environments.

"We're essentially making the system integration of sensors into plant

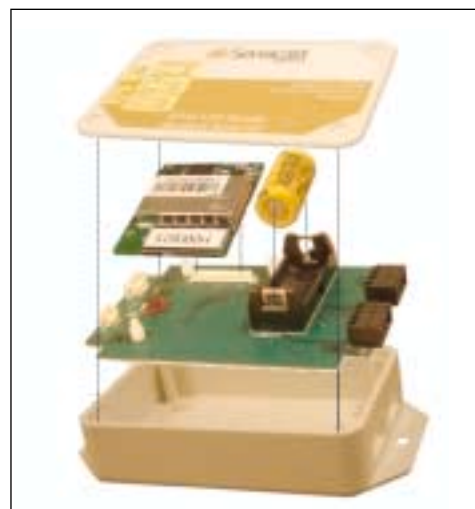
management and control a very simple exercise," said Paul Sereiko, chief executive officer at Sensicast (Needham, Mass.).

The Modular Interchangeable Networking Device (Mind) is "a modular package into which you can insert a number of boards—either 900-MHz or 2.4-GHz radios," Sereiko said. I/O boards then serve as an interface to various sensing devices, he added. Currently, I/O boards are available only for resistive-temperature devices with 0- to 10-volt or 4- to 20-milliamp interfaces.

While Sereiko considers the Zig-

Bee protocol adequate for a range of applications, "it has really focused on cheap, cheap, cheap," he said. ZigBee wasn't optimized for robustness, Sereiko said, which is where the SensiNet protocol comes in. Using frequency hopping on top of the direct-sequence, spread-spectrum 802.15.4 radios, the protocol allows the network to hop among any of the 16 channels available to the 802.15.4 radio. "This allows it to operate in environments that are very challenging for wireless," he said.

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Sensicast's modular package allows developers to insert either 900-MHz or 2.4-GHz radios.

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 **TEXAS INSTRUMENTS**



Modeling standard opens ESL doors

By Richard Goering

Santa Cruz, Calif. — A transaction-level modeling standard for silicon intellectual property will roll out this week that promises to bring chip designers above the register-transfer level. The Open SystemC Initiative's proposed standard is finding strong support among developers at companies like Philips Semiconductors and STMicroelectronics.

"Lack of a standard is preventing companies from exchanging or reusing models from other companies or third-party suppliers," said Ralph von Vignau, CTO of Philips' Reuse Technology Group. New intellectual property (IP) developed within the company will be expected to follow that standard, said Vignau.

The SystemC transaction-level modeling (TLM) standard 1.0 defines application programming interfaces (APIs) and a library that implements a foundation layer upon which interoperable transaction-level models can be built. It is designed to facilitate intellectual-property (IP) sharing and reuse, foster EDA tool development and make it a lot easier for electronics OEMs to use TLM.

Creators of transaction-level models today have to develop company-specific ways of implementing them, said Adam Rose, chairman of the OSCI steering group. The new standard, he said, "moves TLM from advanced users to mainstream users, because the overall investment is quite reduced."

Frank Ghennasia, OSCI TLM working group chairman, said the standard will "open the market for IP providers to supply transaction-level models and be sure those models can be integrated into an SoC [system-on-chip] and into EDA tools. That wasn't possible before, because each company had its own transaction-level models."

STMicroelectronics is migrating its proprietary SystemC TLMs toward the OSCI standard, said Philippe Magarshack, central R&D group vice president for design automation and libraries. "The TLM OSCI standard allows many EDA

vendors to have a viable market by supporting this flavor of SystemC more efficiently, and therefore it allows our SoC developers to be better supported by productivity tools," he said.

EDA vendors that endorsed the OSCI TLM standard in the statement announcing its release include Atrenta, Cadence Design Systems, Calypto, Celoxica, ChipVision, CoWare, Forte Design Systems, Mentor Graphics, Summit, Synfora and Synopsys. Also on board is the Open Core Protocol International Partnership

and run much faster.

There are three TLM levels: untimed, timed and cycle accurate. In ST's experience, said Magarshack, untimed TLMs run 1,000 to 10,000 times faster than RTL, the timed but not cycle-accurate models run 100 to 1,000 times faster and the cycle-accurate models are 10 to 100 times faster.

Magarshack said ST uses transaction-level models for functional IP/SoC verification, early embedded-software development and SoC architecture definition, employing a "model once, use

TLM interfaces, along with object-passing semantics. The API includes a user layer, a protocol layer and a transport layer.

It's important to note that the standard provides only a foundation layer. IP providers will need to provide APIs for specific bus standards, along with TLMs of their IP. They thus create what OSCI's Ghennasia called a "second adaptation layer," upon which system and semiconductor IP can be constructed.

"The OSCI TLM standard does not specify how the foundation calls should be used to model a bus protocol," said Pete Hardee, director of solutions marketing at CoWare Inc. "That is why CoWare has been working closely with the OCP-IP to show that the Open Core Protocol can be modeled on top of the OSCI foundation layer."

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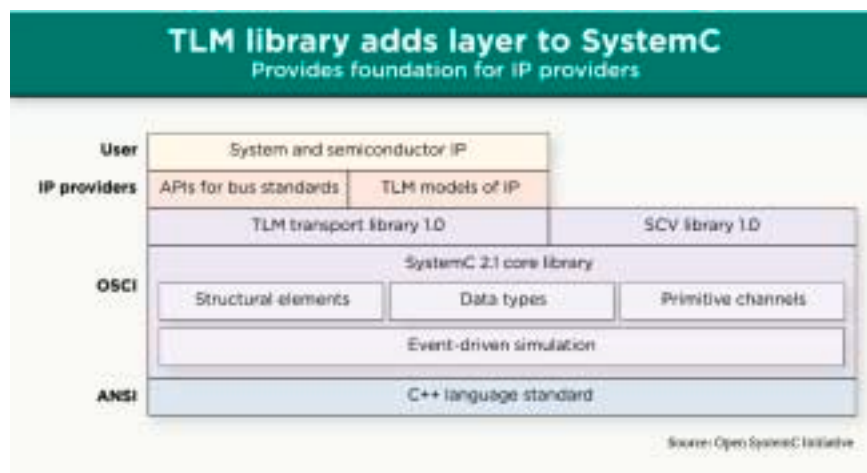
The OSCI TLM standard should work with any EDA tool that implements SystemC 2.1, Rose said.

But Ghennasia said additional tools for monitoring or probing transactions, as well as more automated tools for assembling IP, would be helpful.

Representatives of Atrenta, Calypto, Celoxica, CoWare, Forte, Mentor and Synopsys confirmed with *EE Times* that they currently support the OSCI TLM standard or plan to do so in future releases.

"Today, customers are looking for interoperable system-level IP that runs on EDA platforms of their choice," said Farhad Hayat, vice president of marketing for Synopsys Inc.'s verification group. "OSCI's TLM standard takes a great step toward this by providing a cohesive transaction-level modeling methodology."

Now that the OSCI board has approved the TLM standard, the next step will be to take the technology to the IEEE P1666 committee that's working on the next SystemC language reference manual. Meanwhile, OSCI plans several activities at next week's Design Automation Conference, including a luncheon panel and a North American SystemC user's group.



(OCP-IP) bus standards organization.

"The new OSCI TLM library makes it possible for designers to write models that connect to each other using standard interfaces," said Robert Hum, vice president of Mentor Graphics Corp.'s design verification and test division. "This will enable both reuse and the increased availability of higher-level IP models."

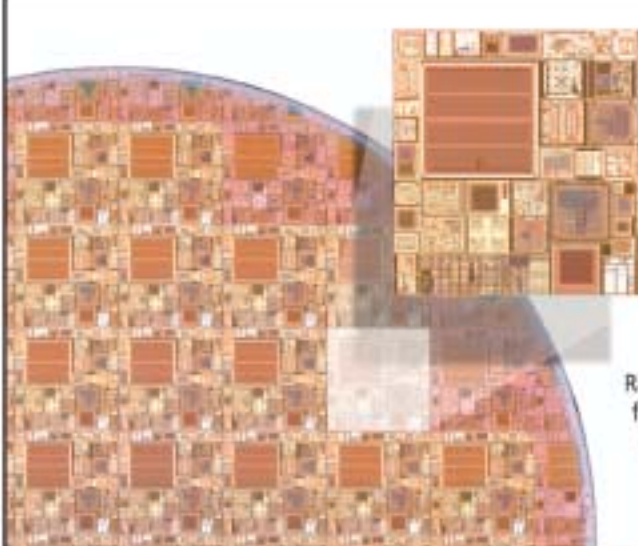
Faster modeling

Transaction-level modeling, said Mike Meredith, executive director of OSCI, is defined as an abstraction level in which communication between modules or threads is handled by function calls. Reads and writes are simple examples. Compared with register-transfer-level models, TLMs require much less coding

many times" methodology. Von Vignau said Philips uses TLM for architectural exploration and software development.

OSCI's Rose observed that TLM is used for hardware/software specifications, for architectural analysis and performance verification and for speeding up RTL verification. "It lives in the space I would describe as system-level verification, between the traditional ESL space and the traditional RTL space," he said. "The TLM standard gives a standard API and methodology that links these domains."

Meredith observed that the TLM standard includes a set of APIs along with a library that implements transports using those APIs on top of SystemC 2.1. To create it, the OSCI TLM working group defined a small set of generic, reusable



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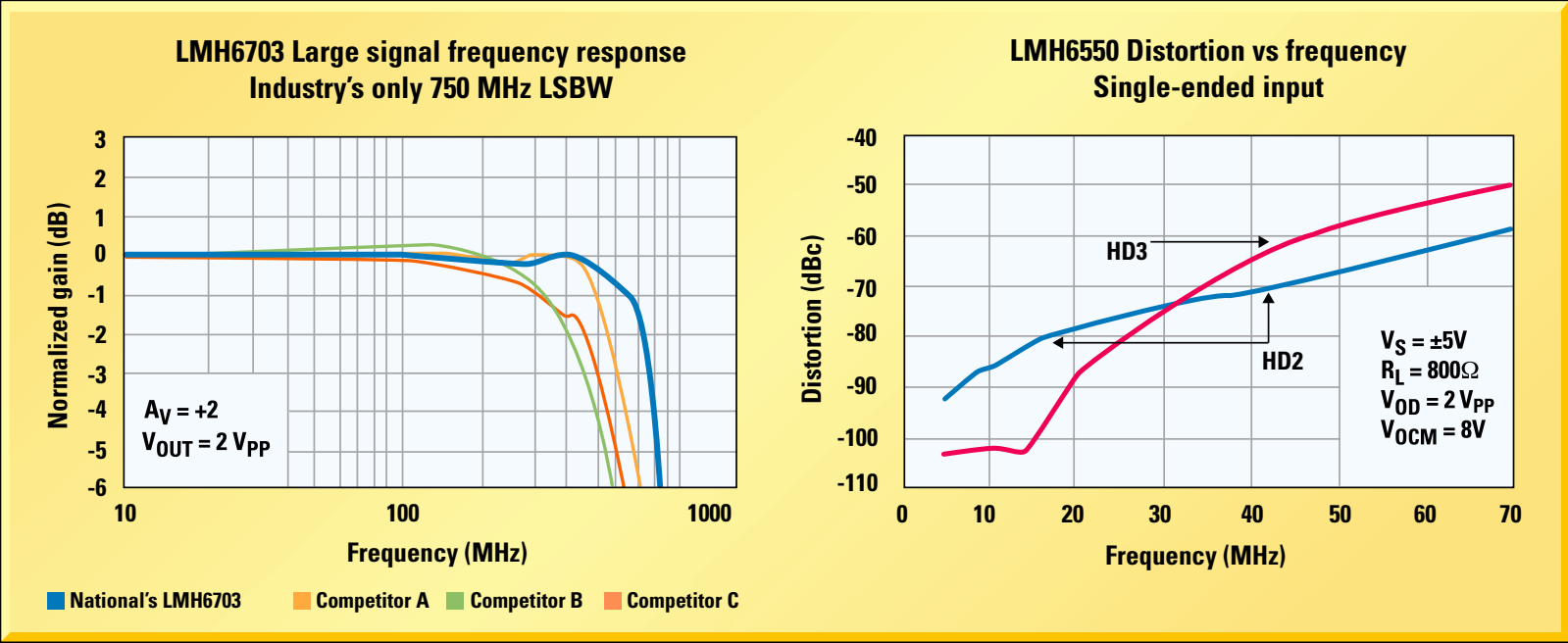
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Woodward Yang

Born:

June 1, 1963, Chicago

Education:

BS, University of California, Berkeley, 1984
SM, electrical engineering/computer science, Massachusetts Institute of Technology, 1987
PhD, EE/CS, MIT, 1990

Work experience:

Professor, Harvard University, 1990-present
Founder, chairman, Silicon7 Inc., application-specific memory vendor based in Seongnam-si, Kyongki-do, South Korea
Consultant to Hyundai, Hamamatsu Photonics, Istituto per la Ricerca Scientifica e Tecnologica, MIT Lincoln Laboratory

Awards and grants

National Science Foundation Young Investigator Award, Army Research Office Young Investigator Award (both 1992)
Phi Beta Kappa, Eta Kappa Nu, Tau Beta Pi (1984)
Three patents: Nos. 5,113,365, 5,214,274 and 5,838,272



CLAYTON M. CHRISTENSEN

Clayton M. Christensen

Born:

April 6, 1952, Salt Lake City

Education:

BA, economics, Brigham Young University, 1975
M.Phil., applied econometrics, Oxford, 1977 (Rhodes Scholar)
MBA, Harvard Business School, 1979

Work experience:

Professor, administration, Harvard Business School, 1990-present
Chairman, president, co-founder (1984), Ceramics Process Systems Corp.
Consultant, project manager, Boston Consulting Group, 1979-84
White House Fellow, 1982-83

Books:

Seeing What's Next (2004)
The Innovator's Solution (2003)
The Innovator's Dilemma (1997)

Make disruption work for you, prof duo says

Best-selling author Clayton Christensen has spent the better part of a decade using his theories about the nature of business disruption to help managers cope with change. Now the Harvard Business School professor has joined forces with Woodward Yang, a colleague at Harvard's Division of Engineering and Applied Science, to bring his analytical approach to the electronics world through a road map document (excerpt, page 26) and a research program. The unique project, directed by Christensen and Yang, is designed to draw semiconductor industry executives to a six-month program that will help them understand the framework for disruption and how they can apply it to their businesses to create profitable new growth. The two sat down recently with editor-in-chief Brian Fuller at Christensen's office in Cambridge, Mass.

EE Times: You two have written a treatise, "Sustaining Profitable Growth," as a starting point for a fall project here at Harvard for semiconductor industry executives. What was its genesis?

Woody Yang: The semiconductor industry is hitting a wall, it's going to break up and face disruptions pretty seriously. Technologically speaking, I remember when 1-micron design rules were going to be the end of the world. And they blew through that. But we're starting to see other factors coming into play: It's too expensive; what do we build? Where do we put all the transistors? People are so focused on the design rules that it just doesn't seem right to me technically. In the business world, it's definitely not the right thing.

EET: Is there really growth to be found in semiconductors per se or is there growth in biocircuits, for example?

Yang: Technology's gotten incredibly powerful. We used to agonize over shrinking 10 transistors into four. Today no one cares. What we use it for is kind of overshoot.

So, what is the future of semiconductor technology? We'll find other uses. That means [using] disruptive technology for other markets. Maybe the things we're using semiconductors for today can be used more efficiently. By the same sense, maybe some of the biocircuits are getting more powerful, so maybe we make a watch out of biocircuits. There definitely will be disruption here.

CONTINUED ON PAGE 22

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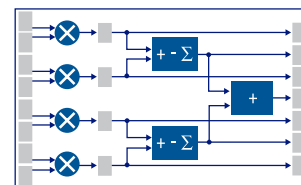
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The interview

Disruptive duo

FROM PAGE 20

EET: Are the leaders in this next disruptive phase going to come from biosciences, for example, or from the semiconductor world?

Clayton Christensen: In one stage of the value-added chain, where the industry is moving toward commoditization, the next layer in the chain will be moving toward decommo-ditization, so there's always an opportunity for proprietary growth right next to where the opportunity is disappearing. For example, it's quite clear that historically there were a thousand, ten thousand, microprocessor designers. The ability to design a microprocessor resided in a limited number of highly skilled people.

The ability becomes more and more rules-based and commoditized. So in the future, somebody's going bring the technology to software engineers, where there will be orders-of-magnitude more people and the technology will allow them to custom-configure processors to optimize every application they're writing software for. That's disruption. Whoever brings that ability, there's a big growth opportunity there, even though commoditization threatens growth on the other side.

Yang: You see similar things in the memory market. DRAM is a commodity. But as it becomes more of a commodity you see more fragmentation—low-power DRAM, high-speed DRAM, DDR-2, DDR-3. You see this commoditization of the memory cell and the core, but you see the specialization of the I/O.

It used to be the instruction set of a microprocessor was very proprietary, very difficult to do. Now there are fantastic tools out there from many companies and ARM licenses you a core for \$10,000 or \$50,000. Now, what's the trick? Can you optimize the microprocessor to be as cheap and as low power and efficient for your application? That's where the proprietary aspect of the microprocessor is coming back, much to the chagrin of Intel and AMD.

EET: Is China a disruption?

Yang: China still has to play by the same general rules that people are playing by in this technology landscape. What's disruptive technology in the United States will be disruptive in China as well. China has very large government policies, so you might see some political strategic advantage to subsidizing their industry, for example, which would have a big impact on the semiconductor industry.

Christensen: Back in the 1960s, the Japanese economy was growing and the Japanese steel companies were just killing the American steel companies. When you read the explanations in *Business Week*, they showed these graphs of the technologies that became available in the early 1960s—continuous casting and basic-oxygen furnaces. Each of those technologies reduced the cost of making

steel by about 15 percent and that means if you adopted those technologies in your steel mill, you could make steel at 30 percent lower cost than the old technology.

The Japanese had been much more aggressive in adopting these new technologies than the Americans. The aspersions that were cast on the sluggish, inward-looking, nonvisionary American managers were just really vindictive, almost. And the praise heaped on the Japanese managers was just flowery. One day it hit me: The American steel industry had not grown since the mid-1950s. Plastics were competing with steel and the auto industry was flat. The last green-field steel mill had been built in 1957, before these new technologies became available.

Between 1962 and 1979, [the Japanese] built 23 new green-field steel mills. When you're building a new mill, you incorporate the latest technology, which in their case was continuous casting and basic oxygen. You can extend the whole advantage of the Japanese in adopting the new technology to the fact that they were growing. So one of the scariest things about China is they're growing and building new fabs. The abil-

'There's always an opportunity for proprietary growth.'

ity in those fabs to reconfigure the processing to be fast, for example, is just a lot easier to do in that format than it is when you just have an existing set of fabs and you have to tear everything out.

Yang: You have to look at how many new design companies there are in China. These companies, I'm sure, are run by people educated in the U.S.—educated in the latest way to design chips, the latest techniques for making RF chips, digital computing chips. In that sense, you're going to see adoption of newer design techniques that will vastly impact the productivity of the industry.

EET: Let's talk a little about cost structures in the semiconductor industry. There's system-on-chip methodologies. Big chips, big expense associated with making them and you need a billion-dollar market to make a decent return. Is there a problem with the continuation of the SoC methodology?

Yang: Where the technology is going just makes SoC more and more difficult. The real reason not to do SoC is a business case. Time-to-market is terrible. Tooling costs are high. When you manufacture, yields are low. You have to manufacture in huge volumes to get yield up and then amortize your tooling costs. And then, how many big markets are there? Let's say it's Nokia buying the chips and they want to buy them at 5 percent gross margin to you and you say,

CONTINUED ON PAGE 24

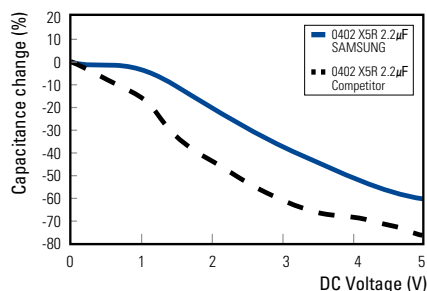
0603 X5R 10 μ F, 0402 X5R 2.2 μ F, the Highest Capacitance



Description	Samsung Part Number
0603, X5R, 10 μ F, 4V	CL10A106MR8NNNC
0402, X5R, 2.2 μ F, 4V	CL05A225MR5NNNC

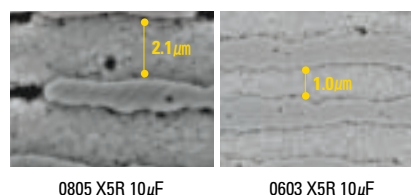
※ X5R : -55°C to 85°C, capacitance change $\pm 15\%$

Samsung Electro-Mechanics has introduced a new 10 μ F multi-layer



ceramic capacitors (MLCCs) in a 0603 case size and a 2.2 μ F version in a 0402 case size, with much stabilized capacitance under the DC bias.

Both of Samsung's latest MLCCs boast the highest capacitance under



the DC voltage conditions for their respective case sizes. The company employs 0.2 μ m grain size technology that results in the outstanding capacitance stability against DC bias voltage as well as raising the breakdown voltage.

Samsung is in step with the electronics industry trend toward slimmer

and smaller designs. These new MLCCs are at least 33% smaller than other Samsung capacitors that offer the same characteristics, fueling expectations of a rapid market changeover to these new Samsung MLCCs.

Samsung already has the technology to handle 100 nanometer fine powder, form a 1 μ m dielectric layer, and stack over 800 layers within a single MLCC. Therefore, the company is well positioned to continue coming out with the world's highest-capacitance MLCCs and maintaining its' market dominance.

0805 X6S 10 μ F with Better DC Bias Performance

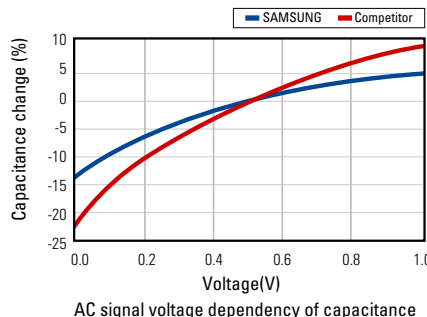
Description	Samsung part Number
0805, X6S, 10 μ F, 6.3V	CL21X106KQQNNNE

※ X6S : -55°C to 105°C, capacitance change $\pm 22\%$

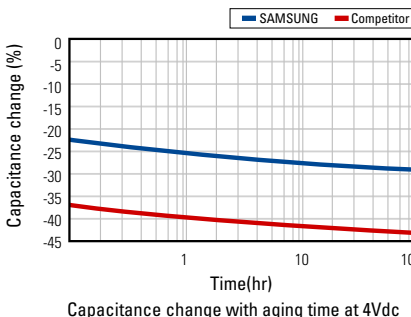
Samsung Electro-Mechanics has completed development of a 0805 X6S 10 μ F MLCC with a very small fall-off in capacitance induced by DC bias voltage.

The capacitance value of an MLCC is inversely proportional to the thickness of the dielectric layer. This requires the layers to be thinner as the case size is reduced and the capacitance is increased.

However, since the electric field



strength per each dielectric layer gets inversely proportional to the dielectric thickness, thinner dielectric layered MLCCs experience stronger electric



field. As a result, capacitance stability against DC bias voltage deteriorates. This phenomenon has required MLCC makers to develop the high capaci-

tance MLCC with less loss of capacitance against DC bias. Samsung's new 0805 X6S 10 μ F MLCC addresses this requirement.

This new product features a tremendous improvement in capacitance reduction by DC bias voltage as time elapses.

After 100 hours under 4 DC bias voltage at 85°C, this product loses only 30% of capacitance. It also showed outstanding capacitance stability with changes in AC voltage. The product can be operated in temperature as high as 105°C.

Polymer Tantalum Capacitor for Mass Production



Market demand for low-ESR capacitors is increasing, prompting Samsung to begin producing tantalum capacitors that employ a conductive polymer in place of the conventional MnO₂ electrodes.

Samsung already has a full lineup of sizes : 2012 (P case), 3216 (A case), 3528 (B case), 6032 (C case) and 7343

(D case), and the leading items being made by the company are the 6.3V 10 μ F (P case), 6.3V 22 μ F (A case), 6.3V 100 μ F (B case), 10V 100 μ F (C case) and 6.3V 220 μ F (D case).

The polymer tantalum capacitor has a maximum ESR value of 30m Ω , which is between half and one-tenth the ESR value of the capacitors with MnO₂ electrodes. As a result, they exhibit outstanding decoupling and noise elimination capabilities.

Samsung is scheduled to start up mass production of these new products in the second quarter of this year.

Low-profile Tantalum Capacitors Developed

Samsung continues to respond to the needs of electronics manufactur-



ers, who are looking to reduce the bulkiness of their finished products.

Recently, Samsung introduced tantalum capacitors in 3216 (A case) and 3528 (B case) sizes but just 1.2mm thick, down from the conventional 1.6mm and 1.9mm thicknesses of the conventional versions.

The company has already completed low-profile versions of the 6.3V 33 μ F (A case) and 6.3V 47 μ F (B case) models and will go into mass production in the first half of this year. Also, Samsung will expand its low-profile lineup using conductive polymers this year.

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SAMSUNG
ELECTRO-MECHANICS



Disruptive duo

FROM PAGE 22

ugh, this just isn't going to work.

I believe that SoC is a case of technology overshooting. I can make 20-nanometer transistors, but is that the right thing to do? Maybe going to system-in-a-package is the way to go. You can deliver almost the same cost structure and much faster time-to-market.

EET: Because of complexity and because the sweet spot right now for China's fabs is 0.18 micron, do you see disruption coming in lower-cost models away from the bleeding edge?

Yang: Today we're saying, "I've stuffed my computer as much as I can with DRAM. I've got the fastest processor in the world at 4 GHz, but Windows is still running slow. Why should I pay more money for it?" People in the industry are saying that if you use SoC, you'll get another factor of two in per-

formance. Well, you always have to have a leading application to pay for technology development. Maybe 0.18 micron is good enough. And yeah, [the chip is] a little bigger, but I care about saving another \$50.

EET: Will the Chinese have enough discipline to stay off the bleeding edge in semiconductors over time?

Christensen: The fact that you start simple and go complicated, and go for higher and higher margins and higher and

higher performance, is not bad news. It's good news. A low-cost strategy is only viable as long as there's a high-cost competitor around. The Chinese will come in at the low-cost, low end of the market and as soon as they've driven the high-cost players out of that simple, tiered market, boom! Pricing will collapse. Then it'll just be low-cost Chinese player vs. low-cost Chinese player. The only way they can keep their profitability healthy is if they move up-market and pick on a high-cost competitor again. They have no options if they want to stay profitable.

EET: Clayton, your first book on disruption, *The Innovator's Dilemma*, came out in 1997. Eight years later, has the United States built a culture of understanding disruption?

Christensen: It's more a culture of misunderstanding than understanding. I don't know whether I made a mistake in calling it "disruptive technology." The word disruptive has so many prior connotations in the English language. A lot of people, without even studying it, heard the term, thought it was good and twisted it to fit whatever pre-existing concept of radical innovation they had in their mind. Most of what's been practiced and studied of this sort is really radical, sustaining innovation. It isn't disruption. Real disruption is, how do you take really sophisticated technology and make things simple and low-cost so that a whole new population can own things and do things?

Yang: I don't think there are a lot of people who understand the frameworks of disruptive technology. But now you look at bio-x, it's a way of taking advanced technology and seeing do these technologies have applications in other areas? The technology becomes disruptive in that area. So there is a mixing of ideas and cultures.

EET: Does the International Technology Roadmap for Semiconductors help the industry understand disruption?

Yang: I believe the ITRS standards are extremely important ways to get people to work together technically. But I think the time has come for technical collaboration to go on to some collaboration about how business models work. Suppliers are suddenly becoming slaves to their customers or customers are being held hostage to their suppliers. While they may cooperate on a spec, they may worry, "Am I screwing myself? I agree to the Jedec DRAM spec. Oh my God, there are now going to be five low-cost manufacturers in China and I've suddenly given away all my IP [intellectual property]."

EET: What's the idea behind the six-month seminar on the future of the semiconductor business?

Christensen: Part of my mission is to help the leaders of industry not get caught by disruption. The evidence is really frighteningly clear that we're getting disrupted. The current group of people [in management] are struggling with it. We want to get to the point where entire management teams get it.

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MP2354	380kHz	4.75 - 23	2	SOIC8
MP1593	385kHz	4.75 - 28	3	SOIC8

Featured Synchronous Bucks				
Part	Frequency	V _{IN} (V)	I _{OUT} (A)	Package
MP2104	1.7MHz	2.5 - 6	0.6	TSOT23-5
MP2109*	1.0MHz	2.5 - 6	2x 0.8	QFN10 (3x3)
MP2105	800kHz	2.6 - 13.5	1.5	QFN10 (3x3)
MP1570	340kHz	4.75 - 23	3	SOIC8

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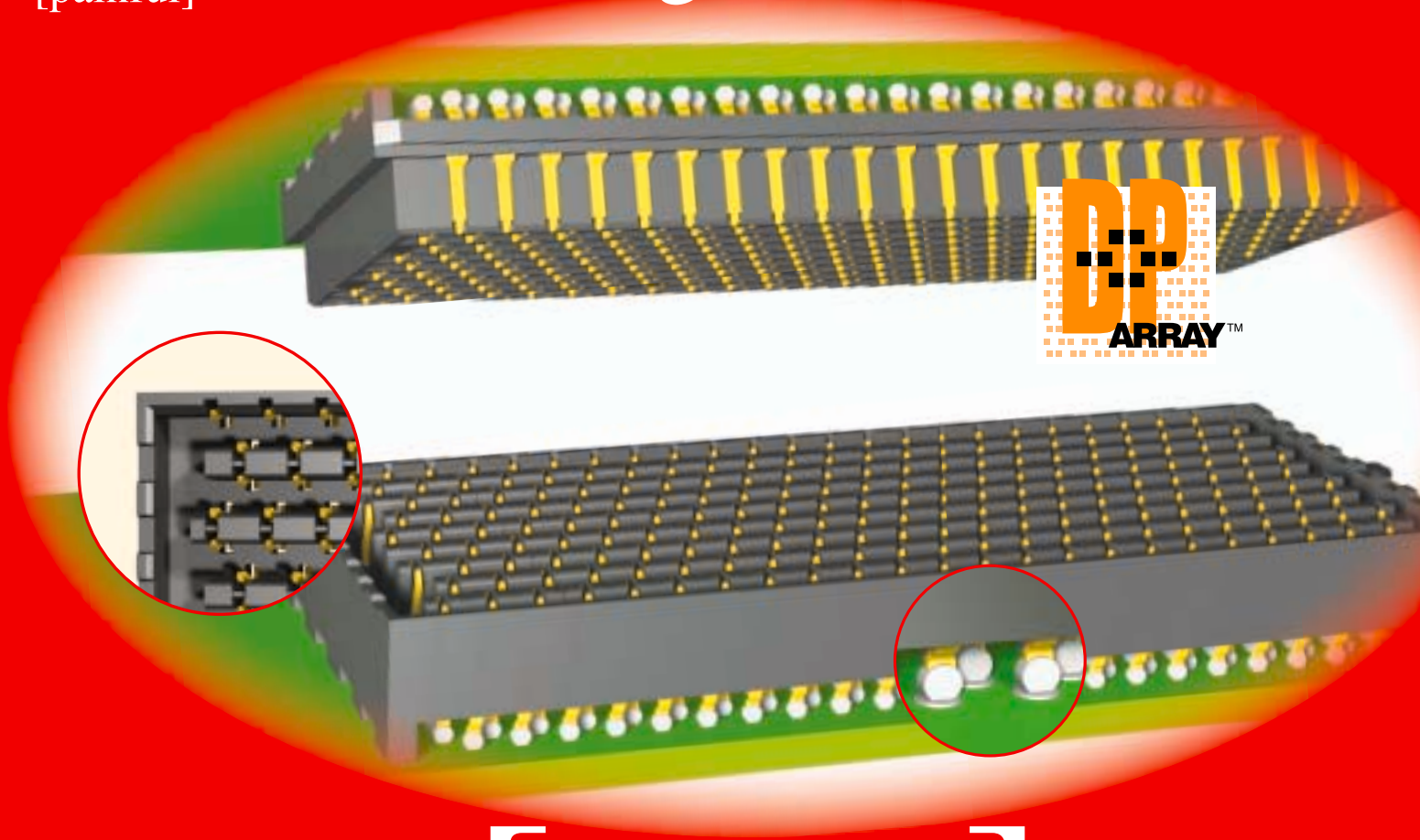
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Commentary: Surviving Disruption

Chip industry must learn not to overshoot

Harvard's Clayton M. Christensen and Woodward Yang (see *The Interview*, page 20) have teamed with consultants Matthew C. Verlinden and Steven M. King of Innovo Inc. to devise a framework for managing disruption in the semiconductor business. The treatise, titled "Sustaining Profitable Growth in the Semiconductor Industry," is excerpted here for the first time.

The semiconductor industry was born out of disruption—the disruption of the vacuum tube by the transistor. While the first transistors weren't very good when compared with the vacuum tube and therefore could only be used in a very limited number of low-performance applications, the commercialization of transistor technology had two characteristics essential to the success of a disruptive technology. First, the technology could be improved at a fast enough rate to satisfy more-demanding applications in existing markets. Second, and as important, profitable new business models were created that could be wrapped around the technology. As it is often applied, the term "disruptive technologies" is a misnomer. Technologies, in and of themselves, are not inherently disruptive. It is the business model wrapped around the technology that makes a technology disruptive.

It is ironic that an industry born out of disruption, an industry that has had almost unparalleled technological advancement and value creation, is now facing disruption to its value chain on a large scale—disruption caused, to a large extent, by the technological advancement of the industry. For a very long time, the almost single-minded focus on technological performance improvement fueled growth and profits for the semiconductor industry. But today, across the entire value chain, that is no longer true. Technology is still critical, but the signposts that something is now uniquely different are everywhere.

Using the disruptive-innovation and value-migration frameworks, the fundamental changes in the nature of competition in the semiconductor industry can be more clearly understood, and future changes in where value will be created and how it will be captured can be accurately predicted.

Just as the International Technology Roadmap for Semiconductors helped the industry set a pragmatic technological vision for the future, the frameworks of disruptive technologies and value migration can help set a business-model vision for the future for both the industry and

individual companies. Understanding how value will be created in the future, how value will migrate and what business models will be required to capture value in the future is possible—a priori.

To be sure, there are future growth and profits to be had in the semiconductor industry. And billions will undoubtedly be spent on investments in search of new growth and profit. But will these investments pay off? By applying the disruptive-technologies and value-migration frameworks, in combination with deep industry knowledge and experience, a global business-model road map can be created to increase the probability that these investments will prove to be profitable. Let's look at the disruptive-technology model.

Probably the most daunting challenge in delivering growth is that if you fail once to deliver it, the odds that you ever will be able to deliver it in the future are very low. This is the conclusion of a remarkable study, "Stall Points," which the Corporate Strategy Board published in 1998. It examined 172 companies that had spent time on *Fortune's* list of the 50 largest companies between 1955 and 1995. Only 5 percent of these companies were able to sustain a real, inflation-adjusted growth rate of more than 6 percent across their entire tenure in this group. The others reached a point at which their growth simply stalled, to rates at or below the rate of growth of the GNP. Stalling is understandable, given our expectations that all growth markets become saturated and mature. What is most alarming is that of all these companies whose growth had stalled, only 4 percent were able to reignite their growth even to a rate of 1 percent above GNP growth.

To understand how the disruptive-technology and value-migration frameworks can be a powerful tool for new growth and profits, it is important to understand what drove the research work behind the frameworks. One driver was the search for answers to these questions:

- How is it that good companies—the kinds that managers have admired and try to emulate, the companies known for their abilities to innovate and execute—fail?
- Why do good managers—earlier praised by their employees, shareholders, the business press, etc.—fail to provide the leadership necessary to sustain success?
- In case after case, how is it that managers who were aware of the disruptive technology that led to their company's downfall viewed the technology as trivial?

The simple answer is that the world changed but the companies leading their industries did not. Executives failed to notice or interpret the signposts of change without benefit of the disruptive-technology framework. The signposts were disregarded as "just part of the cycle" or anomalies that had no larger meaning.

In every instance where seemingly innocuous technology sets in motion the

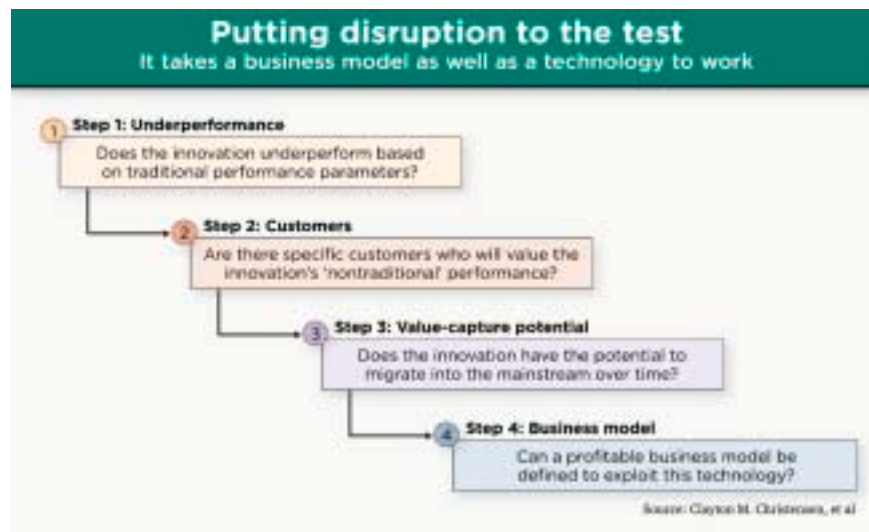
events that cause leading firms to fail, the trigger of disruption and of value migration is when companies supply more performance to the market than the market is willing to pay more for. This event—performance overshoot—sets in motion a series of events that often leads to the disruption of incumbent firms and large-scale change across an industry.

Performance overshoot allows companies with lower-cost business models to enter the market with "good enough" technology that incumbents cannot hope to compete against on a price basis. Incumbents often become trapped by past success: What had worked before will work again. Once performance overshoot has occurred, new performance parameters, such as convenience and customization, become more important. Purchasing decisions are no longer primarily made based on traditional performance parameters.

try incumbents may fall on hard times, new sources of growth and profits will emerge. Companies must figure out the level of traditional performance that is necessary to satisfy the market, while also understanding the level of performance sufficient to gain competitive traction as the basis of competition shifts. Successful companies then would create the right business model for growth and profitability.

The disruptive-innovation model also tells us that this shift of customer preferences to convenience and customization will have ramifications throughout the semiconductor value chain.

What the semiconductor industry has achieved in pursuing Moore's Law over the past 35 years is remarkable. But the very things that fueled the industry's success have created a circumstance in which new business models could reshape the industry. Viewing the semiconductor industry



The industry begins to disintegrate as nonintegrated firms that specialize in one stage or new stages of value enter the market. The business models of many of the industry's leading firms render them uncompetitive in commoditized tiers of the marketplace.

All of these industry-changing triggers have already been set in motion in the semiconductor industry:

- Customers in and of the semiconductor industry are increasingly resistant to paying more for performance increases.
- There is margin erosion in products from PCs to microprocessors to tools.
- Customization and time-to-market emerge as more-critical decision factors.
- Specialized, nonintegrated firms—such as foundries and "fabless" design firms—are displacing integrated firms and beginning to transform the value chain.

Opportunity knocks

The threat of disruption and changes in the basis of competition in the semiconductor industry also gives rise to opportunity. While value will migrate to new areas in the value chain and some indus-

through the lenses of the theories of innovation suggests the future probably will look very different than the past.

When the basis of competition shifts and customers begin demanding exactly the features and functions that they need, they also grow more unwilling to pay for features and functionality that have overshoot their needs. For the semiconductor industry, this will mean that profits in the value chain will shift to new areas of integration focusing on convenience and optimizing performance for an end use.

Using the disruptive-innovation and value-migration frameworks, the seemingly unrelated events taking place in the semiconductor industry come together to tell a powerful story. There is disruption to the industry's value chain on a large scale, and it is already in motion. But the frameworks also tell another story—a priori.

Despite the challenges, value will continue to be created and captured, and its location is predictable. Which companies will see the signposts of change and develop the business models, capabilities and organizational structures to thrive in the new semiconductor industry?

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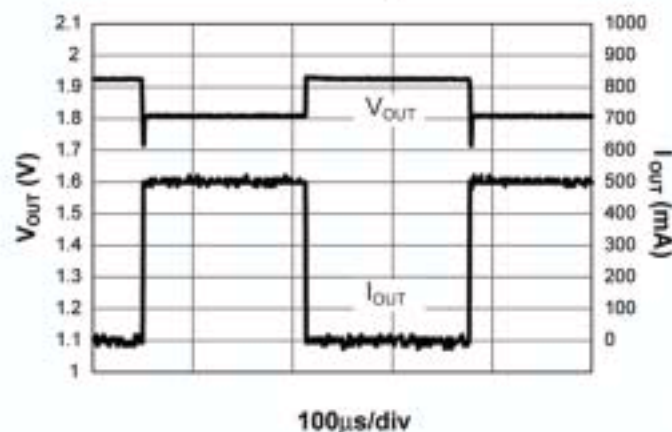
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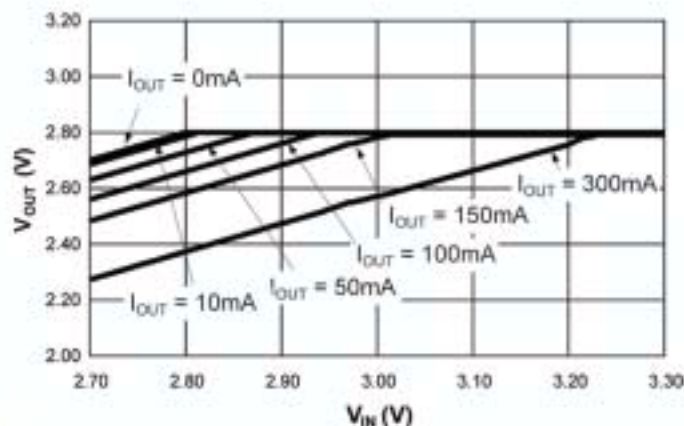
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Wind River

FROM PAGE 12

engineers twice evaluated the Eclipse platform, trying to figure out if the IT-centric technology could meet the needs of the embedded-software community. Development of software for enterprise applications is done in synchronous fashion. Engineers targeting a military system or an automobile often have connections across systems, and software developers must update a register window or a memory window asynchronously.

"The interface must be more messaging based, and for us it becomes a networking problem to send all of these messages back and forth," Evensen said. "So when we set out to develop Workbench, we had to create this asynchronous development system and then bring that knowledge back to the Eclipse community."

Wind River engineers are leading an open-source effort within the Eclipse Foundation aimed at device software development platforms. The group's DSDP committee late last month posted its goals and kicked off a newsgroup at the foundation's Web site (www.eclipse.org).

One advantage of Eclipse, Evensen said, is that partner companies can quickly learn how to develop plug-ins by going to the Eclipse documentation, rather than relying on Wind River engineers to shepherd them through the process. For Wind River, Eclipse's modularity made it possible to tailor the Workbench tools to the needs of the customer. While the Tornado integrated development environment was aimed at the users of VxWorks, Workbench can be adapted to Linux, VxWorks or any other operating system.

"One very nice thing about Eclipse is that you can plug in something that will come into the view without having to recompile," Evensen said. "We can have one product aimed more at the application developers and another one for engineers doing complex hardware bring-up, priced for that segment."

Remote opportunity

CEO Klein worked as a ship-based radar engineer at Hughes Aircraft, and then at Daisy Systems and Daisy-Cadnetix, before spending 14 years in the enterprise software space at Mercury Interactive Corp. (Mountain View, Calif.). He said he wants to apply revenue opportunity lessons he learned in the enterprise software world, including remote diagnostics and debug, to Wind River.

In the enterprise IT sector, Klein said, services such as fault management and remote diagnostics have created a \$14 billion industry, with companies such as Tivoli, BMC, NetIO and others forming around the opportunity. Klein said that in the embedded world, "there is a complete vacuum of those kinds of devices."

To that end, Wind River will develop technology obtained from the recent

Purchasing pieces

Company has been shaped by 15 acquisitions since 1998

	Company	Type, terms	Summary of what was acquired
1-24-05	RTI (ScopeTools division)	Asset Purchase, \$10M	Visualization, dynamic debugging and code coverage tools
10-10-01	Telenetworks	Asset Purchase, \$5.6M	Embedded networking software products
5-4-01	Berkeley Software Design Inc.	Software Asset Purchase, \$23.4M	Robust Unix-based operating systems for embedded devices
4-18-01	Eonic Systems N.V.	Software Asset Purchase, \$15.5M	Digital signal processor (DSP) technology
10-18-00	Dragonfly Software Consulting	Asset Purchase, immaterial	Consulting company engaged primarily in architecture engineering work
10-24-00	Rapid Logic Inc.	Purchase, \$57.5M	Advanced device management technologies for networking equipment and other intelligent devices
7-14-00	ICESoft AS	Purchase, \$24.6M	Innovative embedded Internet browsing technologies for intelligent devices
5-9-00	AudeSI Technologies Inc.	Purchase, \$52.4M	Embedded Java-based tools and other components for building flexible, multiapplication consumer devices
3-31-00	Embedded Support Tools	Purchase, \$331.6M	Integrated hardware and software tools for programming, testing and debugging embedded systems
3-15-00	Integrated Systems Inc. (ISI) 1991 • Software Components Group 10-31-95 • TakeFive Software 1996 • Case Tools Inc. 1-5-96 • Doctor Design 7-29-96 • Epilogue Technology 9-17-96 • Diab Data Inc. 1997 • BetterState 1999 • Software Development System	Pooling. Each outstanding share of ISI common stock was exchanged for .92 of a share of Wind River common stock.	Embedded systems software for a broad range of industries including telecom/datacom, consumer electronics, automotive and aerospace
6-30-99	RouterWare Inc.	Pooling. Each outstanding share of RouterWare common stock was exchanged for 1.82731 shares of Wind River common stock	Portable networking protocol source code
4-7-99	Xact Inc.	Asset Purchase, immaterial	Networking software technology that underlies both advanced switches and routers
7-7-98	Zinc Software	Pooling. Wind River issued 339,917 shares of common stock in exchange for all of the outstanding stock of Zinc	A uniquely powerful, cross-platform graphical user interface (GUI) to the embedded market
2-2-98	Objective Software Technology	Asset Purchase, \$6.1M	Object-oriented visualization technology
1-8-98	Network Computer Inc.	Technology Purchase, \$10M	Comprehensive graphics technology

Source: Wind River Systems Inc.

purchase of the ScopeTools Division of Real-Time Innovations Inc. "It is a difficult technical challenge to remotely debug running systems that you can't stop—for example, a basestation," CTO Evensen said. "The old model of setting a breakpoint and stepping through doesn't work. The ScopeTools help to debug

River tools on a project-by-project basis. And Klein wants customers to take advantage of Wind River "service teams" to supplement the customer's in-house software engineers.

In a move that speaks volumes about its newfound confidence, the 23-year-old company is trying to change the very language used to describe its industry segment. Instead of "embedded software development," Wind River prefers "device software optimization."

The DSO moniker is part of an effort to distinguish between the "old" model, in which a systems company purchases various software tools and then stitches them together in-house, and a new one in which Wind River serves as a "strategic development partner" for systems companies. Klein said the engineering teams at Wind River's customers need to concentrate on developing the applications code—a challenge that is doubling in size this year and next—and partner with Wind River for the tools needed for "software optimization."

"We want to join an ecosystem and provide services on the fly," said Bruggeman, the chief marketing officer. "The question is: How do you price for software in a hardware-centric world? The software model is different than the hardware model."

Daya Nadamuni, a senior analyst at Gartner Dataquest (San Jose, Calif.), said the Wind River managers have their work cut out for them. Regaining trust within the software development community takes time, and previous management "cost the company a lot of good will" with its public opposition to Linux, she said.

"I can't blame [Wind River co-founder] Jerry Fiddler, but he and the CEOs there didn't see the magnitude of the change that Linux brought to the industry," Nadamuni said. At the same time, she added, "the company is still very strong technically."

Competition in the approximately billion-dollar DSO industry is intense, with Green Hills Software Inc. (Santa Barbara, Calif.) attacking the aerospace segment and Microsoft Corp. growing fast in the consumer market.

"In the end, they will be judged by where the dollars are going. That is how people in this industry cast their votes," Nadamuni said.

Wind River's fiscal 2006 got off to a good start. On May 25 it reported a quarterly revenue increase of 17 percent, compared with the first fiscal-2005 quarter. Sales rose to \$61.8 million and the company earned a \$1.8 million profit, compared with a loss of \$3.8 million a year ago.

'With Eclipse, you can plug in something without recompiling.'

—CTO Evensen



without stopping the target."

Klein said Wind River's revenue is now growing at a 30 percent clip, more than double the industry's overall growth rate. Wind River has embraced a subscription model for selling its tools, betting that it can convince the top engineering managers at large companies to use its software throughout their engineering teams, rather than buying Wind

SID displays fruits of OLED research

Apps envisioned from HDTV to handhelds to lighting

By Nicolas Mokhoff

Boston — The LCD juggernaut hasn't halted advances in organic LEDs for flat-panel displays. Technical papers and demonstrations here at SID 2005, the Society for Information Display conference, showed that OLEDs are increasing in size and diversity and that they are being considered for applications ranging from HDTV screens to replacements for incandescent and fluorescent lighting.

The number of organic LED suppliers grew from six in 2003 to 21 in 2004, with Samsung SDI Co. Ltd. the leader in both shipments and revenue, according to market research firm DisplaySearch (Austin, Texas). Samsung presented a slew of technical papers at SID and showed off a 40-inch diagonal HDTV prototype that it called the first single-sheet, 40-inch active-matrix display with a wide-screen WXGA (1,280 x 800-pixel) format.

OLED emissive display technology can be used in passive- and active-matrix displays. For the most part, passive-matrix OLEDs target mobile-phone subdisplays, car audio displays and MP3 players. Volume shipments of active-matrix OLEDs are low due to low backplane yields, but that hurdle should be overcome this year, leading to higher volumes in 2006, according to DisplaySearch.

Progress in OLED technology is as much about materials and design as about successful manufacturing techniques. "OLED Manufacturing Equipment," a newly released report by market research firm iSuppli Corp. (El Segundo, Calif.), provides a searchable database of some 50 OLED equipment makers and their products. It also profiles key deposition equipment suppliers and surveys panel makers about how well equipment functions in the field.

"We set out to analyze the state of OLED manufacturing and how it affects the development of the market," said Kimberly

Allen, director of display technology and strategy for iSuppli.

Three companies—Universal Display Corp. (UDC; Ewing, N.J.), Cambridge Display Technologies Ltd. (Cambridge, United Kingdom) and Eastman Kodak (Rochester, N.Y.)—hold a majority of OLED patents.

At SID, UDC announced development of what it said is the first high-resolution, active-matrix transparent OLED (AM-

Samsung SDI demonstrated its 40-inch AM-OLED prototype at SID and said it is gearing up for mass production of AM-OLEDs next year. It recently concluded a patent license agreement with UDC to use the latter's OLED phosphorescent material and related technologies. The phosphorescent material can deliver bright and crisp images with low power, thanks to an efficiency that's about four times higher than conservative fluo-

to contain the OLED material within the pixel area. The commonality between LCD and OLED backplane fabrication greatly reduces costs and mitigates scaling risks through the use of existing fabrication capacity, the team said.

One remaining hurdle for large AM-OLEDs is operating life. While advances in metal and glass encapsulation technologies have extended the life of AM-OLEDs in mobile displays, the goal of at



TOLED). The display uses the company's phosphorescent OLED and transparent OLED technologies, along with amorphous silicon backplane technology developed at Kyung Hee University (Seoul, South Korea). UDC envisions full-motion video displays providing transparency when turned off in such applications as architectural vision glass, entertainment, medical and industrial products, and helmet shields for the military.

The company also demonstrated a 120 x 160-pixel quarter QVGA, 200-dot/inch monochrome AM-TOLED.

Meanwhile, researchers from Samsung SDI reported on using AM-OLEDs for large HDTV screens. According to Samsung, AM-OLEDs offer many advantages over LCD or plasma technologies for HDTV, promising thinner, lightweight displays with a wider viewing angle, faster video speed, higher brightness and lower power consumption than LCDs at full-color operation.

cent materials, the company said.

At SID, another research group from Samsung Electronics, together with Dupont Display (Santa Barbara, Calif.), described collaborative work on what the team called the "largest full-color, amorphous-silicon, TFT-based, solution-processed active-matrix OLED display." By combining an amorphous-silicon thin-film-transistor architecture and solution-processed OLED emitters, the researchers believe they have achieved the most cost-effective method to date for producing large OLEDs in volume.

"At 14.1 inches, we have broken the 10-inch size barrier and have taken a definitive step toward realizing the mass production of OLED televisions," the teams reported.

Their TFT backplane architecture is identical to that used for LCD backplanes through the first five masks. An optional, sixth mask is used to create the wall layer

least a 40,000- to 50,000-hour lifetime for HDTV panels remains elusive.

Smaller displays

Progress in smaller OLEDs was reported by AU Optronics Corp. (Hsinchu, Taiwan), where researchers have enabled the display of different images on both sides of a 1.5-inch full-color AM-OLED panel controlled by a single IC driver. The double-sided display has high potential in mobile applications, especially in cell phones, the researchers said.

While other dual-emission AM-OLEDs present images on both sides of the display, those are mirror images to each other, which limits such displays' use in commercial applications wishing to display two independent images.

Today's cell phones with dual displays usually use LCDs rather than OLEDs, with a TFT-LCD as the main display and a

CONTINUED ON PAGE 32

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Organic LEDs

FROM PAGE 30

color STN-LCD as a subdisplay; some use TFT-LCDs for both the main and subdisplays. In effect, the module on today's cell phones has two LCD displays physically assembled back-to-back. This makes the module thick, heavy and costly.

The 1.5-inch double-sided AM-OLED developed at AU Optronics has only one backplane, fabricated by putting a top-emitting OLED and its bottom-emitting counterpart on the same substrate. The original subpixel area is divided into top- and bottom-emission regions. By individually driving the top- and bottom-emitting subpixels, two images can be displayed on the panel.

To show the different images simultaneously, an image mixer integrates the pictures and then transfers the mixed image signals to an image processor. The processor marks the mixed image signals by individual scan addresses. The signals are then sent to the IC driver according to the individual scan addresses of subpixels, without any image interference, AU said.

Paint it white

White OLEDs are coming, too. High-efficiency white OLEDs are desirable as an alternative to full-color active-matrix OLEDs because they can be coupled with



Researchers at Kodak are working on white OLEDs, which eliminate the color filter.

color filters to circumvent the problematic shadow mask for RGB pixelation in production and can help achieve higher display resolution, researchers said.

At National Chiao Tung University (Hsinchu, Taiwan), researchers developed efficient top-emitting OLEDs with broad white-light emission. The top-emitting OLEDs have a modified anode and cathode. The researchers effectively removed the ITO layer, shortening the optical length of the device and alleviating the adverse microcavity effect from which a broad emission of white light is obtained.

Researchers at Eastman Kodak are similarly pursuing white OLEDs. At SID, they

described how a highly efficient and stable white OLED enables low power consumption as well as stable emission without use of a color filter.

White OLEDs hold appeal for lighting as well as for displays. At GE Global Research (Niskayuna, N.Y.), researchers are working on large-area white OLED panels that emit 1,200 lumens of illumination-quality light. The researchers explained at SID that general diffuse lighting applications require large OLEDs (greater than 2 feet) in order to provide sufficient illumination and that they must be cost-competitive with today's lighting products.

The researchers used a downconver-

sion approach. A blue-emitting OLED is coupled with one or more luminescent layers, which absorb a fraction of the blue light and re-emit in the green and red spectral ranges. By varying the thickness of the downconversion layers, the composite emission spectrum can be varied to maximize performance for lighting or display apps while keeping the properties of the underlying blue OLED constant.

The architecture divides the device area into smaller emitting elements connected monolithically in series. The required current is controlled by the individual element area rather than by the total emitting area of the device.

The GE team built large-area polyfluorene-based blue OLEDs on 6 x 6-inch glass substrates using the monolithic series architecture. The total area was divided into 144 emitting elements, measuring 1.2-cm². The structure is configured as 12 rows connected electrically in parallel, with each row containing 12 elements connected in series. A 4-square-foot white-light demonstration panel was made by tiling 16 of these white-OLED devices together on a common substrate.

The resulting panel has an average luminance of 1,000 cd/m². The efficacy and total lumen output equate to that of an 80-watt incandescent bulb, and the color quality for illumination exceeds that of fluorescent bulbs, the researchers said.

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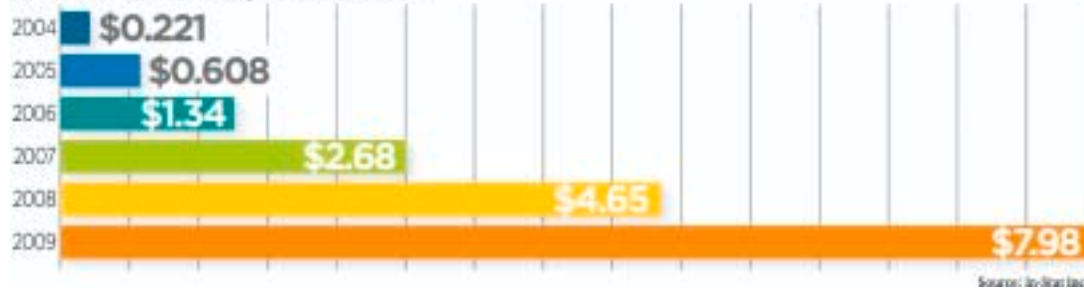
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By the Numbers

Exceptions rule

Advanced TCA revenue, billions of dollars



The general stability of the multifaceted board market obscures some of its bustling segments. The Advanced Telecom Computing Architecture, established by the 600-member-strong PCI Industrial Computer Manufacturers Group as an open standard for carrier-grade networking and communications equipment, will build on its standard foundation and on support from merchant silicon suppliers to expand into military, medical/industrial and enterprise markets, according to "The AdvancedTCA Market Slowly Builds Momentum" report by In-Stat Inc. (Scottsdale, Ariz.). In-Stat projects the AdvancedTCA market to rise at a 104.9 percent compound annual growth rate between 2004 and 2009.



Shipments, year-on-year growth rate

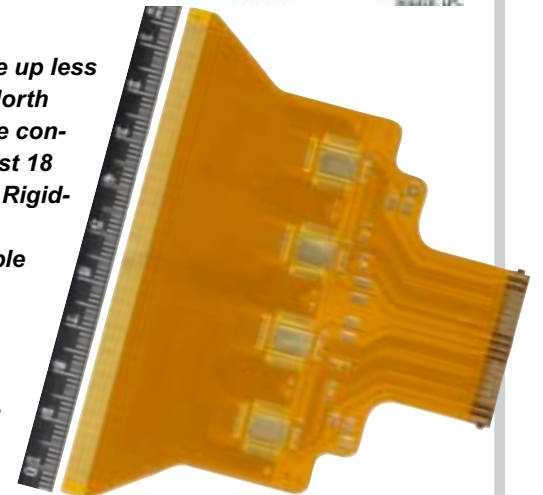


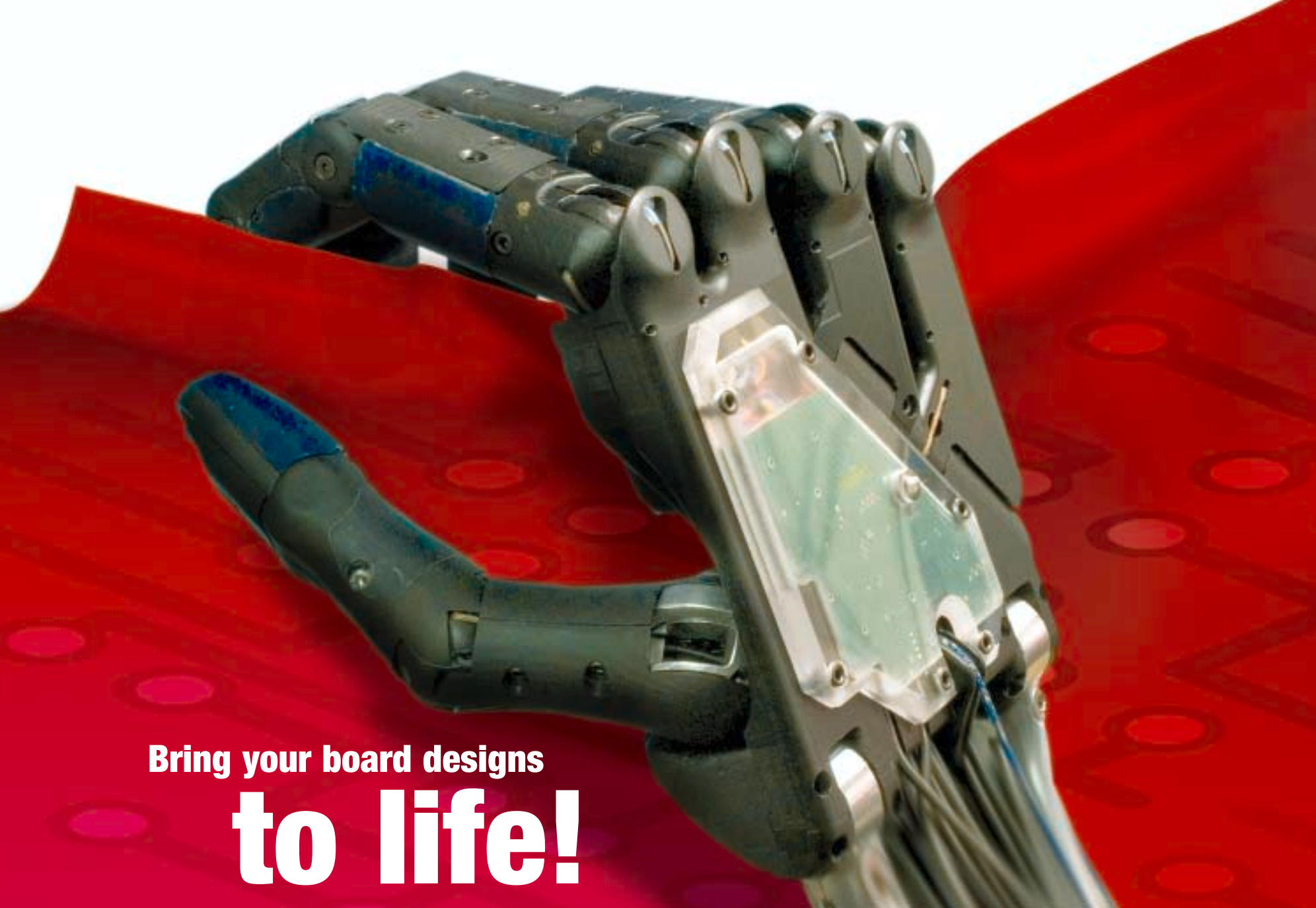
Percentage of growth for boards



The U.S. board market will hold steady over the next few years after 6 percent growth last year. Its growth rates are lower than those for the world market, according to Hayao Nakahara, president of N.T. Information Ltd. (Huntington, N.Y.).

Flexible printed-circuit boards currently make up less than 25 percent of the total board market in North America but have grown at stronger and more consistent rates than rigid pc boards over the past 18 months, according to IPC (Bannockburn, Ill.). Rigid-board shipments in North America increased about 16 percent in 2004 over 2003, and flexible pc boards increased about 67 percent, said Sharon Starr, director of market research for IPC. The trade association's data shows the segments' dissimilar performance. Year-on-year shipments of rigid boards have declined for the past six months, while year-on-year shipments of flexible boards have grown each month since July 2003 and have increased at double-digit rates since October 2003. Rigid boards are normally shipped bare, while flexible boards involve some value-added service such as assembly, Starr said.





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"Song Engine" by Raymond Swanland, from Oddworld Stranger's Wrath videogame

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Patent office rebuts allegations of shoddy workmanship

We are pleased to see that *EE Times* recognizes that the brisk business at the U.S. Patent and Trademark Office (USPTO) is evidence that innovation thrives, and domestic and foreign confidence in the U.S. economy is high ("Documented Innovators," May 16, page 1). Patents are the foundation of the high-tech sector, creating industries and jobs for millions of Americans. *EE Times* is wrong, however, in asserting that the backlog created by the



large growth in the number of innovators seeking to protect their technology with patents "has pressured the patent examiners to process claims faster, which in turn has bred accusations of occasionally shoddy work."

The United States leads the world in protecting intellectual-property rights because quality is paramount at the USPTO. The amount of time an examiner spends on a patent application is not dictated by the amount of work sitting on the shelf. In fact, our backlog is as large as it is because we give our examiners the amount of time they need to do the job right. Examining patents is an inherently intellectual process. The amount of time an examiner spends on a case is dictated by the complexity of the technology, not by how many cases are pending.

We are addressing the backlog in the most appropriate way. We are hiring more examiners. This year, we are hiring nearly 900 new, well-educated, highly skilled examiners. We anticipate hiring an additional 900 examiners next year. Our examiners are some of the best engineers and scientists this country has to offer. They are highly skilled and well-trained to ensure that they continue to offer U.S. innovators the strongest patent protection in the world.

John Doll
Acting Commissioner for Patents
U.S. Patent and Trademark Office
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Employment opportunities must be equal for all

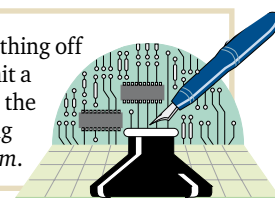
The general vibe I get from Crosstalk letters is that Americans are against offshoring, but the only reason I can see behind it is the attitude of "we don't want to lose our jobs." But I believe strongly in equality and fairness, and the notion of blocking opportunities going international in the mere interest of local job protection discriminates just as much as declaring that people with blonde hair should not be offered engineering jobs. So if I had brown hair and was just arguing things for my own best interest, I should be perfectly content with a law like that, right? Wrong.

Fortunately I try to see things as much as I can without bias. And just as talented blonde-haired people should not be denied a job because of their hair color, other talented people should not be denied a job because of their origin. Who gets hired should be based only on who's best for the job for the price. And just as with contract work, if someone's willing to do the same job for a lower price, then either your demands are too high or you're looking in the wrong place.

Then I see a clear case of hypocrisy: One particular *EE Times* reader, Frank Roso, wrote about imbalances in the global economy. ("Pistorio's world view smacks of noblesse oblige," May 9, page 34). In a statement regarding Pasquale Pistorio, Roso wrote, "I find it odd that he does not even mention the role played by repressive regimes in keeping poor nations poor." Excuse me? Who's the repressive regime? It seems to me that many Americans are crying "foul" when American corporations are offering jobs to engineers in these so-called repressed countries. Very talented engineers, I may add. But should an Indian or Chinese company ever offer a lucrative overseas job to an American, nobody even blinks an eye.

Justin Frim
Technician
Humansystems Inc.
Brampton, Ontario

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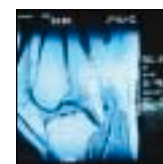
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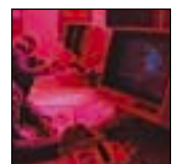
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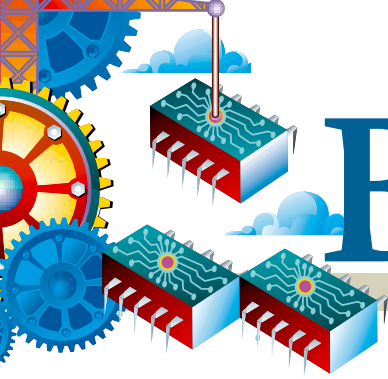
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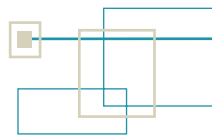


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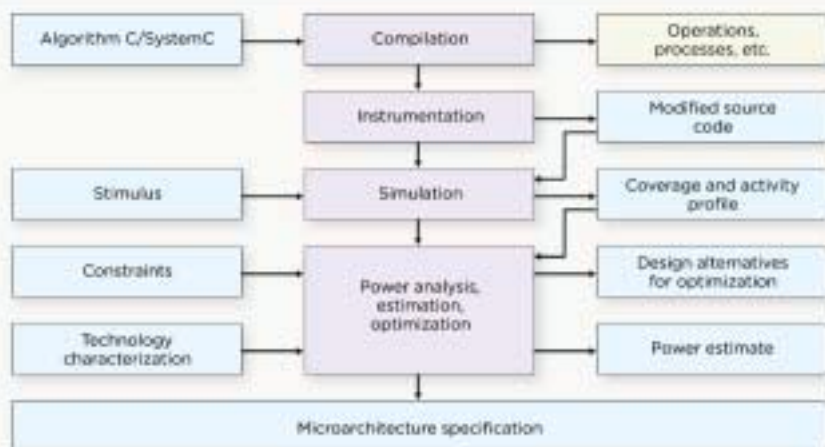


BuildingBlocks



ChipVision adds leakage power estimation

Orinoco product analyzes C algorithms



Source: ChipVision Design Systems

WIRELESS

UWB over power line IC offers speedy option

By Patrick Mannion

Manhasset, N.Y. — Convinced that Wi-Fi is too costly and that existing ultrawideband offerings are a long way from meeting the needs of consumer equipment vendors, Artimi Inc. has announced a UWB chip that it believes solves the dilemma. The company has combined an 800-Mbit/second physical layer based on pulse-position modulation (PPM) with IEEE 802.15 media-access control, promising full-home coverage using both wireless and power line media.

The use of PPM separates the Santa Clara, Calif., company not just from Pulse-Link, which also uses UWB-over-power line technology, but also from the two main UWB approaches: the Wi-Media Alliance's multiband OFDM and Freescale Semiconductor Inc.'s direct-sequence UWB. As such, the entry constitutes a fourth high-speed UWB communications option.

According to Craig Mathias, principal at Farpoint Group (Ashland, Mass.), multiple UWB options may not be such a bad thing. Since UWB represents a "set" of technologies, he said, it is premature to standardize on a single one right now. "The market must

decide," he said. "We're not ready as an industry to make that decision."

Many UWB proponents are concerned that European regulators may impose tighter restrictions on UWB at sub 5 GHz than exist in the United States, or even push UWB above 6 GHz. As defined by the U.S. Federal Communications Commission, UWB can operate from 3.1 to 10.6 GHz.



CEO Macnab: Artimi is aiming for an overall system throughput of 100 Mbits/s at 10 meters.

This is not a problem to Artimi, however, a spokesperson said, since its chip—which currently operates in a single band in the 3- to 5-GHz region—has been designed from the ground up

CONTINUED ON PAGE 44

DESIGN TOOLS

DAC drills down to the system level

By Dylan McGrath and Richard Goering
San Francisco — The emerging electronic-system-level (ESL) design market will be a focus of attention at next week's Design Automation Conference, as vendors roll out solutions for leakage-power analysis, transaction-level debugging, cost estimation, coprocessor synthesis and multiple-clock-domain synthesis.

ChipVision Design Systems is claiming an industry first with an ESL power opti-

mizer that includes leakage power. Summit Design Inc. is offering a transaction-level-modeling (TLM) viewer that works with SystemC simulators. And Giga Scale Integration Corp. is adding economic analysis to its InCyte chip estimation tool.

CriticalBlue, meanwhile, has added a streaming-coprocessor capability to its Cascade synthesis design environment. And Bluespec Inc. is adding multiple-

CONTINUED ON PAGE 42

DATA CONVERSION

Linearization chip looks to soup up performance

By Stephan Ohr

San Francisco — Startup Optichron Inc. (Fremont, Calif.) will introduce a linearization IC this week for high-speed analog-to-digital converters. The circuit will boost the spurious free dynamic range (SFDR) of converters operating in the 100-Msample/second range by as much as 25 dB.

The company believes its Turbolinear technology can reduce the size, cost and power consumption of high-speed data conversion systems by eliminating many amplification and filter components ordinarily built in to cope with nonlin-

ear distortions. Turbolinear is an adaptive DSP-based technology that mathematically models nonlinear distortions and applies corrective filtering, said CEO Roy Batruni, Optichron's founder.

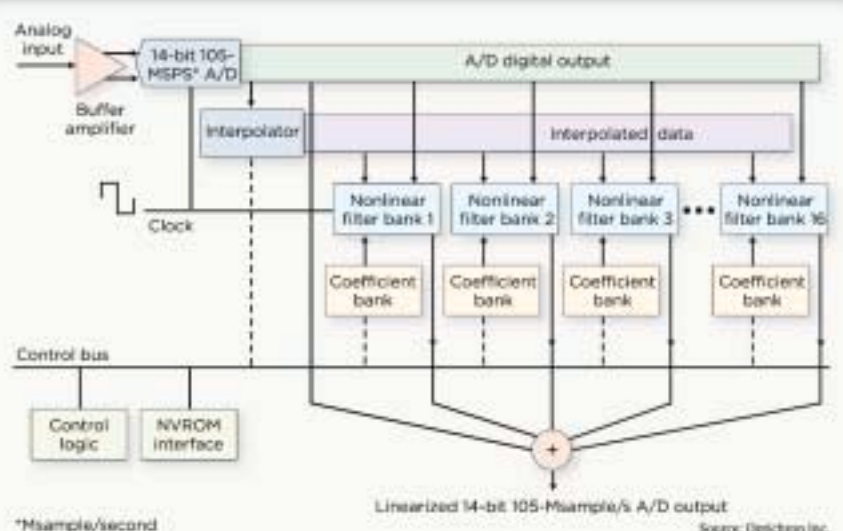
The technology can be applied to all types of nonlinear distortion, including static, dynamic, continuous, discontinuous—and even distortion with memory effects, he said. It is also scalable, allowing engineers to enable or disable filter blocks for specific applications.

By improving the effective bit resolution and SFDR of the signal capture

CONTINUED ON PAGE 44

Optichron pulls out nonlinearities

A separate filter algorithm tackles each type of A/D nonlinearity



Source: Optichron Inc.

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TOSHIBA



DAC preview

FROM PAGE 40

clock-domain support to its Bluespec high-level synthesis tool.

While previous versions of ChipVision's Orinoco power-optimization tool have focused on dynamic power, Orinoco 2005.1 adds power estimation for leakage, which ChipVision says is equally important at the 130-nanometer node and below. Orinoco 2005.1 enables designers to optimize a C

or SystemC algorithm's implementation for low power, said ChipVision CEO Stan Krolikoski. The tool provides an output in the form of an Orinoco microarchitecture indicating how many resources are needed for the implementation of a particular block before RTL coding.

"This is not a pushbutton, 'forget it' solution," said Frank Schirrmeister, vice president of business development for ChipVision. "Orinoco 2005.1 provides the tools for the designer to make optimizations."

The release claims improved accuracy

for both dynamic and leakage estimates, to within 25 percent of gate-level estimates. An automated characterization flow enables the creation of libraries for pre-RTL power estimation.

Orinoco 2005.1 is shipping now. Pricing for time-based licenses starts at \$40,000 per year.

Summit Design, meanwhile, has introduced Vista 1.1, an improved version of the integrated development environment that Summit rolled out in January for SystemC-based analysis and debug. The envi-

ronment's transaction-level-modeling viewer works with a designer's SystemC simulator to provide a view of system-level design behavior for debug. The tool, which works directly with SystemC code, promises to eliminate the time-consuming manual code instrumentation that Summit says has historically been necessary in SystemC design environments.

An understanding of Open SystemC International's SystemC is built into Vista to reduce the workload on developers, said Summit president and CEO Emil Girczyc.

The Vista TLM viewer allows direct observation of the key attributes of SystemC TLM, such as time, kernel cycles, return value, function attributes, structure and concurrency, the company said.

Vista 1.1 will be available in the third quarter. Vista 1.0 is currently available on the Linux platform, with a one-year time-based license beginning at \$5,000.

Giga Scale Integration this week will roll out what it claims is the industry's first comprehensive IC economic-analysis engine. It's an add-on to the company's InCyte chip estimation tool. A free version is available at www.ChipEstimate.com.

The InCyte software gives users early estimates of IC die size, yield, power and leakage, and it enables trade-off analysis to be run at a high level of abstraction. While the client software is free, users can get paid upgrades with proprietary data from intellectual-property vendors and foundries.

The new economic-analysis engine provides a budgetary quotation and a return-on-investment analysis that includes the factors built into the final-product cost of an integrated circuit. It also includes an IC life cycle analysis, letting designers forecast and account for mask respins, increasing yields and decreasing wafer and package costs. For "enterprise class" InCyte users who have upgraded to foundry-specific data, pricing for the InCyte upgrade starts at \$2,000 per month.

Synthesis advances

CriticalBlue, which provides tools that synthesize programmable coprocessors, has added a streaming-coprocessor capability to its Cascade design environment. Streaming allows autonomous transfer of data into and out of the coprocessor with minimal CPU interaction.

Cascade lets users offload embedded-software functionality directly into a programmable coprocessor. With the new capability, an autonomous streaming implementation can be chosen for applications in which continuous streams of data are processed, such as audio and video functions. Cascade lets users select the input and output parameters to be treated as streams. It generates the hardware and software interfaces needed to communicate with an existing DMA controller. The streaming-coprocessor feature will be available in the second half.

Finally, Bluespec is coming to DAC with enhanced support for multiple clock domains, along with integrated clock management and formal clock verification. These enhancements work with the Bluespec Compiler, which provides synthesis from SystemVerilog assertions.

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UWB chip

FROM PAGE 40

to support the higher-frequency bands without compromising performance.

The RTMI-100 was designed around the belief that consumer electronics companies are not too concerned about standard solutions, particularly when it comes to point products such as a wireless microphone, said Colin Macnab, Artimi's recently appointed CEO. Instead, they're

concerned about cost and availability.

"The cost of wireless is just too much with Wi-Fi," said Macnab, the former vice president of marketing and business development at Wi-Fi proponent Atheros.

The RTMI-100 is a single chip made in an 0.18-micron silicon germanium process from Chartered. Key to the design is the use of PPM, a relatively simplistic scheme pioneered by the likes of Time Domain Corp. While a PPM design lends itself to a very simple transmitter, high data rates have traditionally been difficult

to achieve due to the extremely tight timing and clock recovery required on the receiver end. That problem spurred many to drop PPM in favor of the direct-sequence or multiband-OFDM schemes.

Artimi has overcome those issues using advanced front-end processing based on a massively parallel DSP front end operating at more than 2.4 teraops/second, said chief technology officer Mark Moore. The PPM receiver performs direct deconvolution of the radio channel, effectively acting as a zero-intermediate-frequency

PPM receiver. The receiver is fed from an on-chip low-noise amplifier and a sampler running at 10 GHz.

The front end is followed by an open-source CPU for the physical-layer (PHY) control, said Moore. While the chip is currently being characterized, Macnab puts the power target at under 1 watt.

The PHY controller is followed by a fully 802.15.3-compliant media-access control. At the back end comes the I/O CPU, a 200-MHz RISC processor that manages the PCI interface and allows the device to control external PCI-connected peripherals such as Ethernet PHYs.

Externally, said Macnab, all that is required to complete the system is a 25-MHz crystal, an additional LNA, a TX/RX switch and an external nonvolatile memory (serial PROM or flash ROM) to hold the device program.

Initial performance figures indicate a PHY capable of 800 Mbits/s or higher, said Macnab, but the company is aiming for an overall system throughput of 100 Mbits/s at 10 meters, he added.

The company said it is shipping samples and expects to move into volume production during the second half. The RTMI100 mini PCI development kit will be available shortly.

Linearization IC

FROM PAGE 40

systems, Optichron's linearization technique can eliminate the harmonics, or "spurs," in the output of an RF receiver/downconverter, for example.

Advanced transceiver sets could reduce the number of symbols required to decipher each data bit (improving data throughput), replacing QPSK modulation with QAM constellations, Batruni speculated—if only the received phase-frequency shifts were easier to detect. They would be, he suggested, if the data capture system produced a more-linear output signal.

Optichron began as a fabless chip maker in January 2003. The Turboliner offering targets not only direct IF receivers but also fiber-optic receivers, communications test equipment, medical image acquisition and military radar processing. Optichron has been showing its devices to a variety of customers that are using 12- and 14-bit data converters operating in the 80- to 125-Msample/s range.

As a proof of concept, Optichron will market three-chip A/D modules. The OM1400 module includes a front-end buffer amplifier, an A/D converter chip and Optichron's linearization IC. There is an A model and T model: The OM1400A is built around Analog Devices' AD6645; the OM1400T module is built around Texas Instruments' ADS5500. Both modules have a signal-to-noise ratio of 70 dB typical and an SFDR of 90 dB. The OM1400A module is sampling now; the OM1400T will sample in the third quarter.

While the company's goal is to market its Turboliner filters as standalone ICs, it has not ruled out an intellectual-property licensing scheme, Batruni acknowledged.



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Migration path	All devices code compatible for seamless upgrade

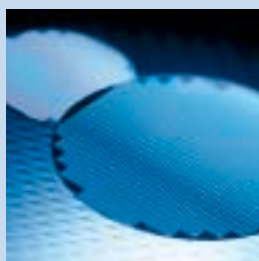


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Never stop thinking.



WIRELESS ICs

Ember samples one-chip ZigBee

By Patrick Mannion

Manhasset, N.Y. — Ember Corp. will use this week's Sensors Expo & Conference in Chicago to launch what it calls the first fully integrated ZigBee chip. By packing the radio, memory, a 16-bit controller and fifth-generation EmberZNet protocol stack on chip, the company promises to speed the time-to-market and lower the cost of ZigBee-enabled devices.

The ZigBee wireless-networking protocol sits atop the physical and media-access control layers of IEEE 802.15.4-compliant silicon (see related story, page 68). The first certified platforms recently emerged from Chipcon, Freescale, Ember and CompXs (which has since been purchased by Integration Associates). And Atmel and others are lining up their own introductions.

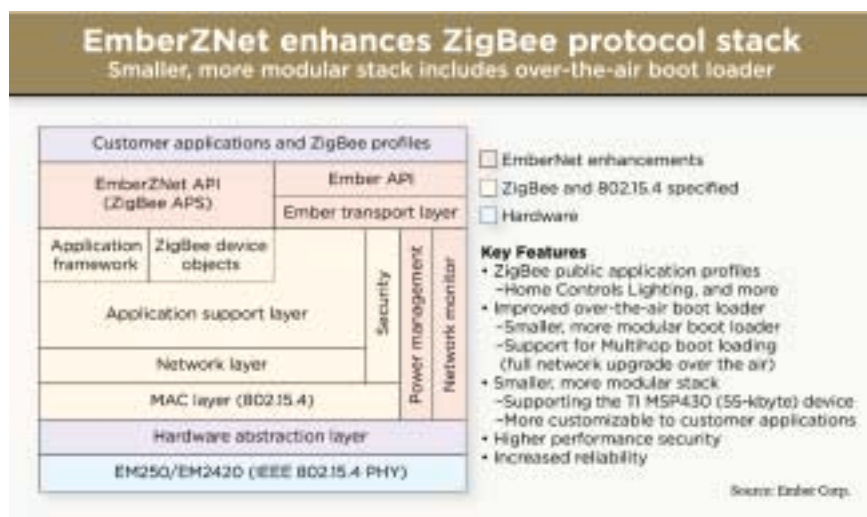
"There will be three to five major suppliers of ZigBee solutions, along with some that will use the 802.15.4 standard with their own proprietary protocol on top," said Farpoint Group principal Craig Mathias.

In November, Chipcon AS announced

the 2430 as the first single-chip ZigBee offering. But the 2430 has yet to ship and is not listed on Chipcon's Web site. Thus Ember (Boston) is laying claim to being first with its EM250.

The device incorporates the full RF chain, with 128 kbytes of flash and 5 kbytes of ROM. The RF chain is a departure from the company's previous generations, the technology for which was licensed from Chipcon. Instead, the chip was designed from the ground up by U.K.-based Cambridge Consultants Ltd. (CCL). Ember acquired CCL's ZigBee team and intellectual property in March 2004.

Ember paired the RF chain with its proprietary, 16-bit Zap2 controller. Thus the EM250 is a departure from all other ZigBee offerings to date, which have centered on 8-bit, 8051-compatible MCUs, said chief software architect Zachary Smith. Designers still have the option of using an external 8051 and using the EM250 as strictly a communications processor with the ZigBee stack.



The company is announcing version 2.0 of the stack with the EM250. Called EmberZNet 2.0, the improved stack offers the same public application profiles but adds an improved over-the-air boot loader; a smaller, more modular stack;

more security; and improved reliability.

The EM250 is manufactured in a 0.18-micron process and costs less than \$4 in high volume, said Smith. It is sampling now, with volume production set to start in the middle of the third quarter.

FUNCTIONAL VERIFICATION

'Virtual emulation' tool does SoC software models

By Dylan McGrath

San Francisco — Claiming new technology in functional verification, Tharas Systems Inc. will introduce a software-based emulation capability this week along with low-cost additions to the company's line of Hammer simulation accelerators.

Virtual Connect is the first virtual emulation software that is accurate at the register transfer level, according to Tharas. The offering creates software models of system-on-chip platforms. That provides an emulation capability that is customizable, scalable and easily deployed while it facilitates concurrent hardware-software development, according to Tharas. Virtual Connect is also said to eliminate the need for many of the engineering resources traditionally needed for emulation, thereby allowing presilicon SoC platforms and embedded systems to be verified while software is debugged concurrently.

Virtual Connect comes in different application-specific platforms for the graphics, networking and wireless market segments. Each platform is fully customizable, the company said.

The tool is based on a hierarchical architecture that includes a platform layer, protocol layer, link layer and transport layer. The platform layer is designed to deliver the interface to the Virtual Connect end user. The protocol layer provides the interface between the platform layer and the design under development.

The link layer delivers data-management services, and the transport layer

performs various transport mechanisms to transfer data physically between the link layer and the design under development. Users can integrate their platform at any layer of the hierarchy, Tharas said, and do not have to use all layers.

Tharas' other new product, the next generation of its Hammer product line, is designed to be what the company refers to as the industry's first family of "verification appliances."

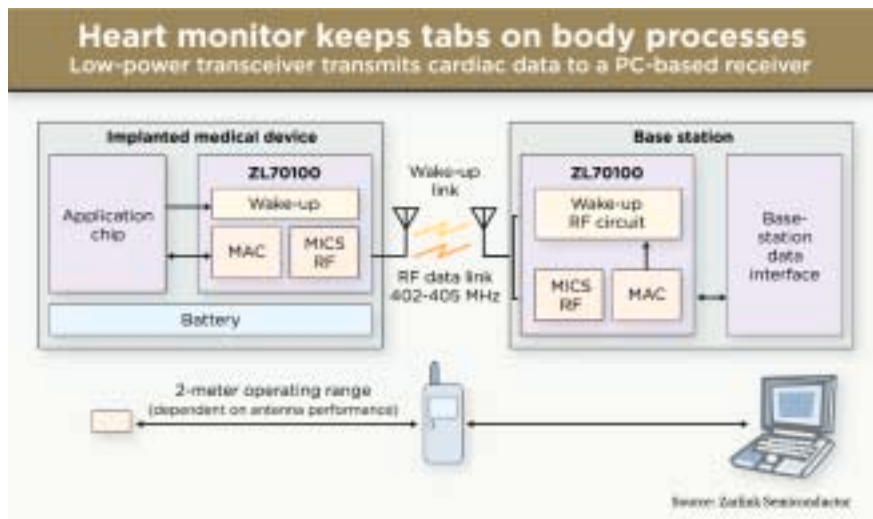
Hardware accelerators, based mainly on their cost of ownership, have traditionally been the exclusive domain of companies with large capital equipment budgets, according to Rich Curtin, vice president of marketing at Tharas. With the Hammer S-Class and M-Class, Tharas is aiming to bring this technology to the mainstream by providing devices that are smaller (the single-user S-Class is rack-mountable), plug into standard power outlets and are less expensive and easier to use.

The S-Class is capable of supporting up to 16 million gates and the M-Class up to 64 million gates, Tharas said.

Virtual Connect supports Solaris and Linux platforms and will be available in July, Tharas said, with a list price that starts at \$75,000 per platform.

Pricing for the Hammer family is based on user configuration, starting at \$200,000 for the S-Class (4 million gates configuration) and \$750,000 for the M-Class (32 million gates configuration).

— Dylan McGrath is EDA online editor for the EE Times Network.



MEDICAL DEVICES

Transceiver low in power for implants

By Stephan Ohr

San Francisco — Zarlink Semiconductor has specifically designed the ZL70100 transceiver chip for medical implants. It operates in the 402- to 405-MHz Medical Implant Communication Service band and targets applications such as implanted pacemakers, defibrillators, neurostimulators and blood glucose sensors.

The transceiver maintains a wireless link between implanted medical devices and outboard basestations. The ZL70100 is capable of entering a "sleep" mode, where it consumes less than 0.2 microamps. Fully "awake" and transmitting data, it consumes approximately 5 mA. Implant batteries—power sources for the device—vary from 1.8 to 3.2 volts.

The device can hit raw data rates up to 800 kbits/second (100 kbits/s with error-correction). Some applications may save battery life by delivering the "payload" in a 500-kbit/s burst mode and then promptly going to sleep, said Steve Swift, senior vice president and general manager of the Ottawa company's ultralow-power communications division. The Zarlink transceiver can send 500-kbit/s data over a typical 2-meter range.



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PHYSICAL IC TOOLS

Three tout more nimble physical design

By Richard Goering

Santa Cruz, Calif. — Three tool vendors are pitching breakthroughs in IC physical design in advance of next week's Design Automation Conference. New products include a fast design-rule checking (DRC) tool, a combined power and signal-integri-

ty signoff solution, and a physical-synthesis suite that takes variability into account.

Magma Design Automation Inc. this week will release Quartz-DRC, which claims to verify any chip design in two hours or less. Apache Design Solutions Inc. is rolling out PsiWinder, a critical-

path analysis tool that considers both power and crosstalk. And Sierra Design Automation Inc. will announce Pinnacle 2.0, which allows concurrent multimode and multicorner analyses of timing, area, power and signal integrity.

Because it promises a next-generation

IC physical-verification solution, Quartz-DRC has been one of the most anticipated products in Magma's Cobra release. The product will attempt to challenge Mentor Graphics Corp.'s longstanding market lead in this sector with its Calibre DRC and LVS (layout vs. schematic) products.

Quartz-DRC technology was originally developed by Mojave Design, a 2002 startup that Magma acquired last year. "Most of the DRC and LVS tools in existence were all designed in the early to mid-1990s," said Mojave founder John Lee, now the general manager of Magma's physical-verification business unit. "That's a long time for EDA tools to be in the marketplace and be unchallenged."

Lee said Quartz-DRC has functionality equivalent to that of Mentor's Calibre or Synopsys' Hercules tools but that it provides that functionality in very different fashion: Quartz-DRC runs over distributed Linux networks in a way that's scalable over 50 or more CPUs.

LVS capability will be handled in a separate product, Quartz-LVS, slated for release later this year. Magma is working on design-for-manufacturability features for Quartz-DRC, but those aren't announced as yet. Extraction is handled separately by Magma's Quartz-RC product or by extraction products in third-party IC layout flows. Also missing is the wealth of foundry rule decks available for Mentor's Calibre. As of now, a TSMC 90-nanometer rule check is available for Quartz-DRC, and IBM has plans for 65-nm support, Lee said.

With its distributed processing capabilities, Quartz-DRC claims to run any design of any size within two hours—provided you throw enough CPUs at it. In one benchmark example, a 200 million-transistor graphics processor with a 13-Gbyte GDSII file ran in 1.5 hours on a network of 50 workstations. Magma claimed that "tool X" took 44 hours in the same benchmark.

But if tool X was Calibre, Joe Sawicki, general manager of Mentor's design-to-silicon division, doesn't seem concerned.

"The only reports we have on Quartz-DRC and -LVS are secondhand from individuals who are not using Calibre's performance features and who are trying to pass off apples-to-oranges benchmarks as valid comparisons of tools," he said.

Lee said Magma has run experiments with Linux networks of more than 100 workstations, and he said the speed of the tool increases linearly as more are added. "Overhead is in the noise," he said. The product does not, however, offer multi-threading for multi-CPU workstations.

Lee said Quartz-DRC has met foundry requirements for accuracy and that the tool is more accurate than existing solutions when it comes to modeling density and chemical-metal polishing effects. That's because it isn't restricted to "windows" of time and can calculate density at any point in a design, he said.

Input includes a GDSII layout file and a foundry rule deck. Although it's completely automatic, the product also has a Tcl interface that allows users to customize rule checks and output text reports, with the ability to cross-probe into Magma or

CONTINUED ON PAGE 52



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PHILIPS



IC physical design

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third-party layout environments.

What makes Quartz-DRC so fast, Lee said, is fine-grained parallelism. "We can take a single DRC job and break it into thousands of smaller jobs, each scheduled on a Linux farm," he said. Also, the tool can process a number of commands simultaneously, on different CPUs.

Quartz-DRC is available now, although Magma has not announced pricing. Quartz-LVS is to follow later this summer.

Combining power, crosstalk

Well before chip designs reach the DRC stage, designers need to verify timing. Enter Apache's PsiWinder, a critical-path and clock tree analysis tool that considers crosstalk and dynamic-power integrity effects on chip timing. It's Apache's first solution to address crosstalk noise, said CEO Andrew Yang. "Because of the impact of noise on timing, it's important to combine power integrity and crosstalk noise analysis," he said.

PsiWinder provides a transient simulation of the dynamic V_{dd}/V_{ss} noise waveforms that come out of the Apache RedHawk dynamic-power analyzer. To do this, it includes 10 licenses of Apache's NSpice product for distributed simulation

over Linux or Unix workstations. PsiWinder's approach is unique, Yang said, because other solutions assume power supply noise is static inside timing windows, instead of taking "time point by time point" noise waveforms.

Other EDA solutions also separately analyze power integrity noise and crosstalk noise, Yang said. "These two sources of noise need to be concurrently handled, and ideally they should be handled at every time step because they are analog noise waveforms in nature," Yang said.

To use PsiWinder, designers must first identify critical paths for analysis. "With something as accurate as true Spice, you cannot traverse every single path in an SoC [system-on-chip] design," Yang noted. In one benchmark, he said, PsiWinder handled around 1,000 paths in an overnight run on 10 CPUs.

Inputs to PsiWinder include V_{dd}/V_{ss} noise waveforms, a Spice netlist and library, the critical paths selected for analysis, and coupled parasitic information (including the full coupling effects). The user does not need to provide any test vectors, Yang said, and "there is no need to hack the Spice netlist."

PsiWinder then launches jobs on multiple machines and comes back with a timing report. Users can also back-annotate results to layout, since RedHawk has chip layout information. "We are working with

quite a few customers who are seriously considering Spice signoff for clock networks and critical paths," said Yang.

PsiWinder, which requires RedHawk, will be available in the third quarter starting at \$150,000.

Design for variability

At Sierra, the new mantra is "design for variability." That means the Pinnacle physical-synthesis tool can concurrently optimize timing, area, power and signal integrity across all operating modes and corners, rather than one corner at a time, as is the case with many existing tools. "We've come up with a way that you can do it all in one shot, rather than having that expensive iteration in the end," said Shankar Krishnamoorthy, Sierra's CTO.

New capabilities in Pinnacle 2.0 include an adaptive variability engine, a "signoff quality" timing analyzer and enhancements to the Detailed Native Analysis (DNA) kernel that underlies the physical-synthesis tool. The kernel now supports multiple operating modes and metal interconnect variations.

A cell phone chip, for example, might have several operating modes, including sleep, standby and active, each with its own timing frequency and constraints. It will also have different process, temperature and voltage corners and, because of on-chip metal variation, interconnect cor-

ners such as maxR (maximum resistance) and minC (minimum capacitance).

The timing engine in Pinnacle has added support for on-chip variation, multiple modes, multiple corners, multiple V_{dd} and complex clocking. While Sierra calls it "signoff quality," it's not meant to replace the widely used Synopsys PrimeTime product, Krishnamoorthy said. Rather, the intent is to bring this implementation timer closer to the level of quality found in final-signoff timers.

The adaptive variability engine accounts for variability at every stage of the design flow and optimizes all metrics concurrently, Krishnamoorthy said. Further, he noted, it allows variability analysis early in the physical-design flow. Users define variability "scenarios" consisting of various combinations of modes and corners. The DNA kernel then does a "one-shot optimization" over all of those scenarios, Krishnamoorthy said.

Sierra, he said, has gone up to 15 or 16 mode and corner combinations in one run. That's possible, he said, because all the scenarios are represented by one timing graph, which he called the "biggest innovation" in the Pinnacle 2.0 solution. Other tools, he maintained, would require a different graph for each scenario.

Pinnacle 2.0 is available now and has already had tapeouts, Sierra said. Prices begin at \$395,000 for a one-year license.

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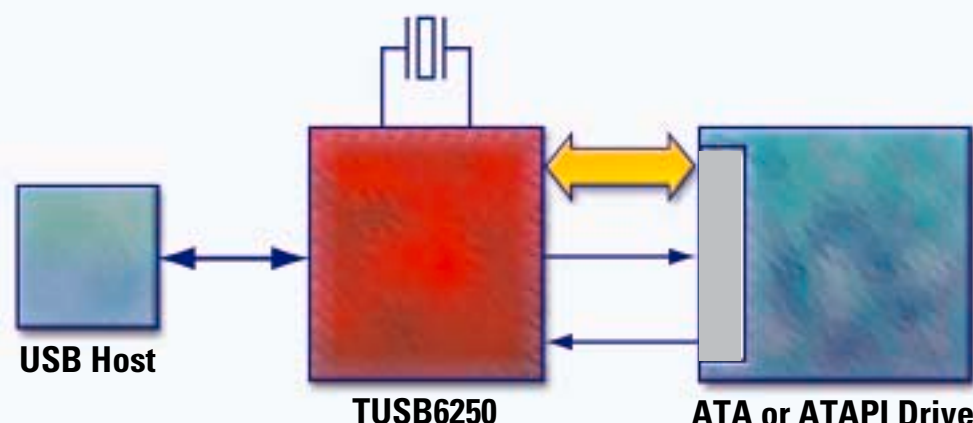
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TUSB3410	Full	3.3	Yes	32-LQFP	\$2.59
TUSB6250	Full, High	3.3	Yes	80-TQFP	\$2.80

USB Hub Controllers

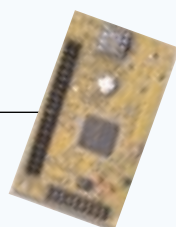
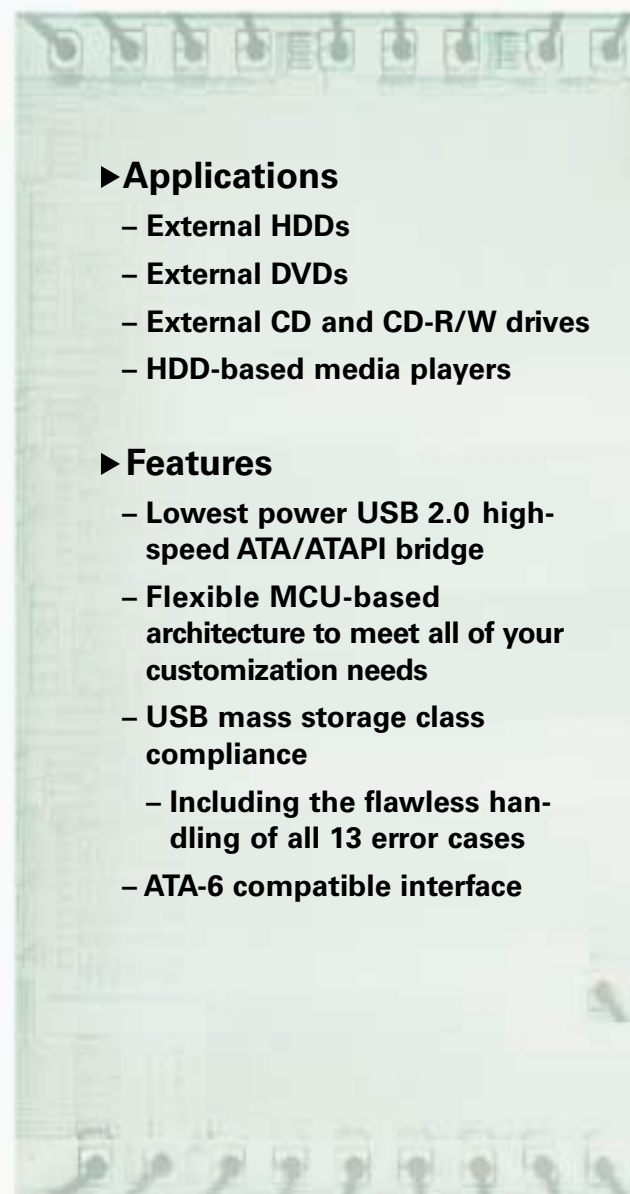
Device	Speed	Ports	I ² C	Voltage (V)	Package	Price Starts at 1K
TUSB2036	Full (1.1)	2	No	3.3	32-LQFP	\$1.15
TUSB2046B	Full (1.1)	4	No	3.3	32-LQFP	\$1.19
TUSB2077A	Full (1.1)	7	No	3.3	48-LQFP	\$1.93
TUSB2136	Full (1.1)	2	Yes	3.3	64-LQFP	\$4.04
TUSB5052	Full (1.1)	5	Yes	3.3	100-LQFP	\$5.06

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 **TEXAS INSTRUMENTS**

ARCHITECTURES

ATCA wares on full display at show

By Loring Wirbel

Chicago — If the sheer volume of support from board developers, semiconductor players and embedded-software programmers is any indication, then the Advanced Telecommunications Computing Architecture should turn the corner to mainstream acceptance at this week's Supercomm.

Embedded computing specialists Motorola Computing Group and Artesyn Technologies will roll out full ATCA product suites at the show. Companies showing reference designs will include Applied Microcircuits Corp.; AudioCodes Ltd. will show reference designs. And Agilent Technologies Inc. will roll an ATCA-specific test environment.

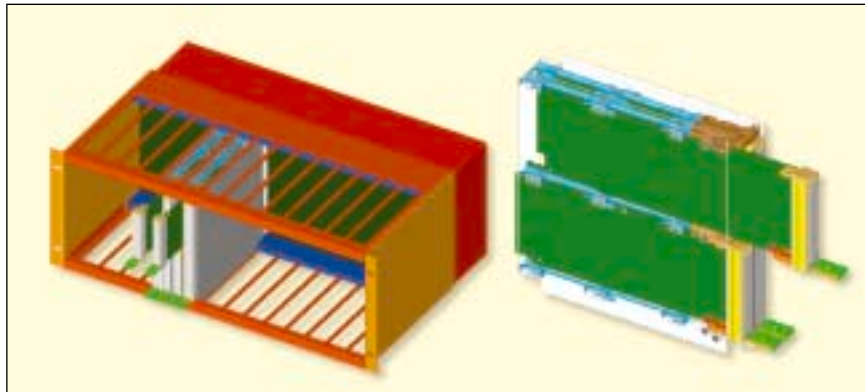
Supercomm 2005 also will represent an ATCA milestone in that it will host the launch of several mezzanine modules meeting the new MicroTCA standard. The Advanced Mezzanine Card (AMC), for one, is a module that will fit into a MicroTCA blade or pod that will allow the ganging of four or eight AMC devices in a chassis meeting ATCA or MicroTCA standards.

John Fryer, director of marketing for Motorola Inc.'s switched platforms opera-

tion, said MicroTCA will find a home in systems closer to the edge of the public network, such as small routers and access devices, Internet Protocol PBX systems and Node B basestation controllers. The full-size ATCA standard will be used in larger

nel, and the Avantellis family, which is similarly configured but offers prebundled software environments from Motorola's NetPlane protocol software group.

Both families are based on a 14-slot 12U chassis, with a switching blade offer-



Artesyn's module allows as many as eight PMC/AMC cards to fit into the 'pod,' or blade.

systems within carrier central offices, such as core routers and soft switches.

This year, Motorola introduced two families of ATCA products—a "naked hardware" version called Centellis, based on dual-Xeon boards and a Linux 2.6 ker-

nel, and the Avantellis family, which is similarly configured but offers prebundled software environments from Motorola's NetPlane protocol software group.

Artesyn's mezzanine-card effort for MicroTCA will begin with a dual-wide Pentium card, the Kosai PM. The card

marries a Pentium with an Intel F7520 north bridge device, a south bridge and support for up to 2 Gbytes of DDR SRAM.

Artesyn will show off an ATCA board that will support up to four mezzanine cards for use in control-plane processing or communication services. The Katana ATCA board supports a dual symmetric-multiprocessing PowerPC. The four cards leverage the PMC configuration but can support a move to AMC in the future. RISC-based processing can be extended through the use of the Katana packet processor blade, which can be expanded to incorporate as many as six PowerPCs.

SENSORS

'Universal' signal conditioner

By Stephan Ohr

San Francisco — Sensor Platforms Inc. (Santa Rosa, Calif.) will use the Sensors Expo & Conference in Chicago this week to introduce what it calls a universal sensor signal-conditioning platform.

Many sensor signal conditioners can handle resistive bridges with multiple impedances, acknowledged George Hsu, president and CEO. But they have trouble with capacitive and inductive loads. Sensor Platforms' SSP1492 sensor signal processor provides the signal conditioning for a range of sensor types including pulse, voltage, current, inductive, capacitive and resistive sensors, he said.

Based on the popular 8-bit 5051 microcontroller, the SSP1492 can serve as a standalone sensor system controller or as the development platform for a wide variety of sensing and control applications. "Applications support is the hot button in the sensor world," Hsu said. "The automotive-system designers get good support, but not the smaller companies—certainly not the garage shops, which are doing some of the most innovative work."

In addition to a positive response from sensor makers, Hsu said the platform is generating interest among manufacturers of cell phone, PDA and gaming platforms interested in using capacitive sensors in place of mechanical thumbwheels.

The SSP1492 is built around a pipelined 8051 processor running at 14 Mips. It integrates math engines and a frequency-mode data converter that has scalable dynamic range, accuracy and speed. The system is said to be capable of taking 32-bit sensor measurements—effectively reading 1 part in 4,294,967,296.

SILICON ENGINEERING

Aiding nanometer-scale design, tool offers multiple-library access

By Richard Goering

Santa Cruz, Calif. — Multiple standard-cell libraries are becoming increasingly necessary for nanometer-scale IC design, but it's difficult for EDA tools to access them. Silicon Navigator Corp. promises to change that with Library Smart, an addition to the its OpenAccess-based Rocket Framework.

Aimed mainly at in-house or commercial EDA developers, Rocket Framework adds Tcl scripting, a graphical user interface, an incremental timing analyzer, schematic and layout visualization and RTL elaboration to the OpenAccess database. The new Library Smart technology provides a way to centralize, organize and manage library data and to capture "best practices" associated with libraries.

George Janac, Silicon Navigator chief executive officer, said multiple libraries are frequently needed below 0.13 micron. Designers often use high Vt libraries to reduce leakage current, but because there's a performance penalty, they'll also use low Vt libraries where performance is critical.

There's also a growing need to run

optimizations across process, voltage and temperature corners, Janac said.

"The main problem Library Smart is designed to solve is how you organize the data and interface these multiple libraries in a way that tools can understand," Janac said. "Today, the data on how you use libraries is all buried in

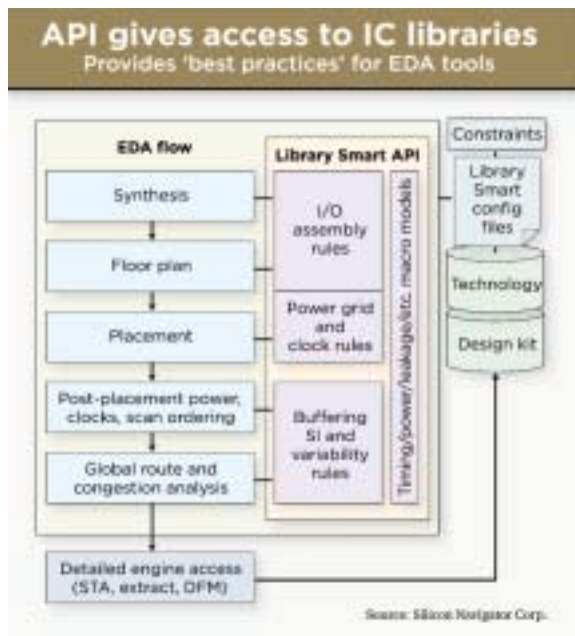
application notes. The user has to read the application notes and know how to trick the tool into doing this interfacing."

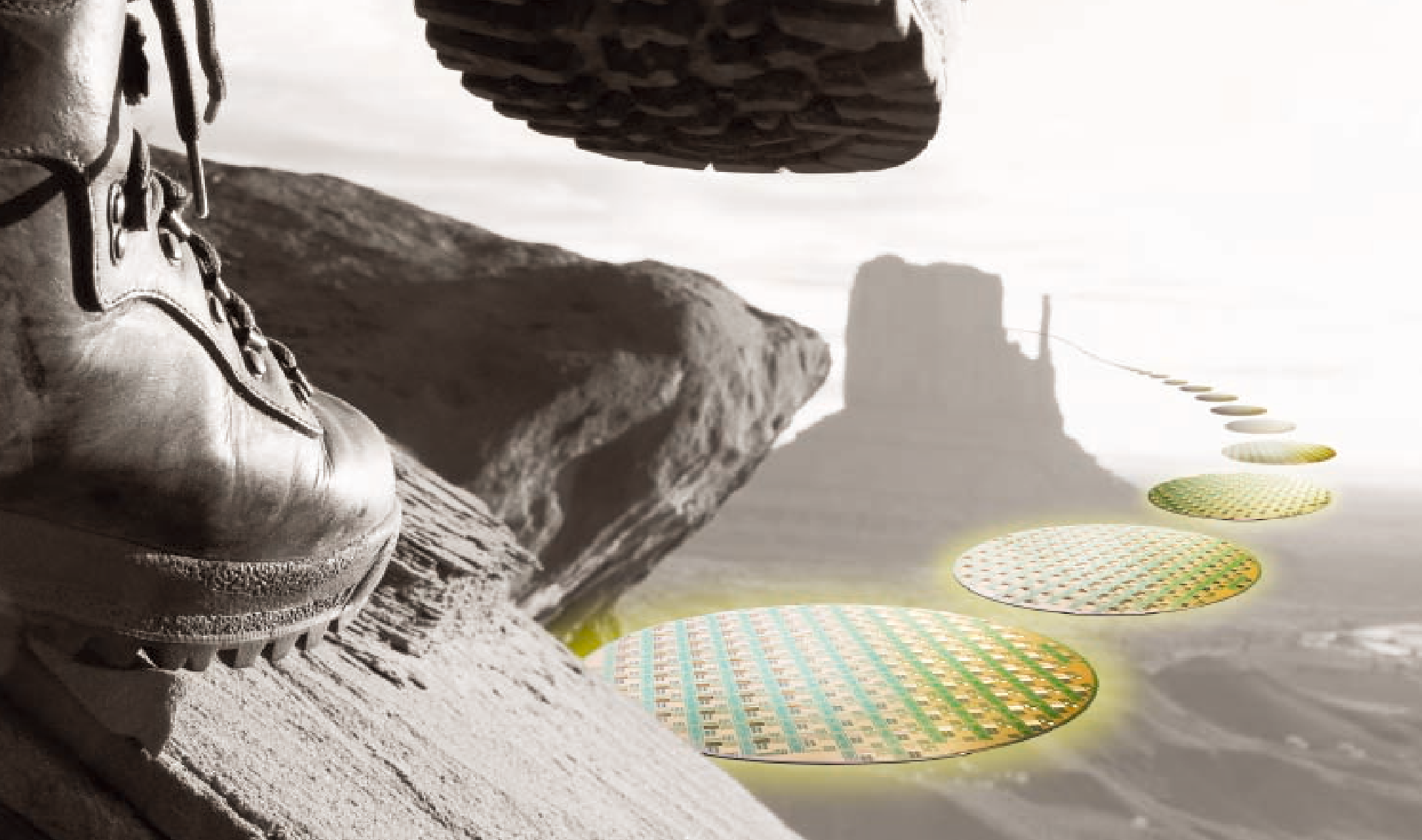
One result is that end users can't do flat designs with multiple libraries, Janac said. "The tools are forcing people to design a block in one library, then design another block, and then interface between them," he said.

Library Smart is a data management and organization tool as well as an API, Janac said. Part of its job is to abstract the library data so optimization tools can grab the only the data they need for a task.

The API extends the OpenAccess data model to give developers access to the library information. It can point an EDA tool to the correct library to use. It also provides access to "best practices" that show how libraries should be used. Vendors and users can encode their own best practices into Library Smart.

Library Smart technology is available now with Silicon Navigator's Rocket Framework. It comes bundled with a C++ API for incorporation into in-house applications. Pricing starts at \$50,000 for development seats.





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Accelerating Silicon Success



'Vision chips' mimic eye, brain functions

By R. Colin Johnson

Portland, Ore. —As the long development of charge-coupled device (CCD) and CMOS active-pixel sensor technology begins to pay off in the form of affordable all-electronic still and video cameras, a second wave of solid-state imaging chips with very different capabilities is emerging from research labs around the world.

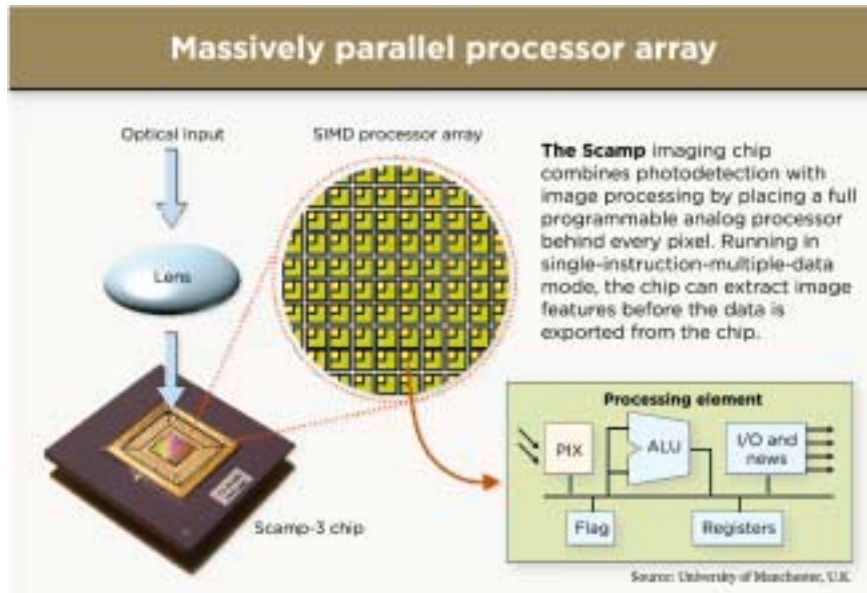
Called "vision chips," these silicon imaging devices are typically parallel computers on a chip implementing a processor per pixel to mimic neural processing circuitry in the retina. Rather than striving for high resolution and faithful color reproduction, vision chips capture other aspects of the eye and brain functions, such as edge and motion detection. Target applications include security systems, autonomous robots, artificial implantable retinas and biochemical analysis.

A few projects have reached the commercial stage, including a real-time in vivo glucose-monitoring system from Array Vision Engineering Co. (Alachua, Fla.) and a security camera being marketed by Pixim Inc. (Mountain View,

Calif.), which has commercialized research from a project at Stanford University (see related story, below).

An example of state-of-the-art vision chip technology surfaced at last month's International Symposium on Circuits and Systems in Kobe, Japan, where EE professor Piotr Dudek of the University of Manchester (England) demonstrated a third-generation device with 16,384 pixel-processors that mimics the retina. Called Scamp, for "SIMD current-mode analog-matrix processor," the chip integrates an arithmetic-logic unit, memory, control logic and an input/output circuit behind each and every pixel. The Scamp-3 vision chip promises to enable robots and automated inspection, surveillance and vehicle-guidance systems to "see" in a manner similar to human sight.

"Our smaller, previous-generation device, the Scamp-2, comprised 1,872 processors and is working very well in the lab," said Dudek. "We had some problems with the fabrication of the Scamp-3 chip, which we believe we have corrected when we submitted it for another silicon run.



We now expect to obtain fully functional Scamp-3 devices in July."

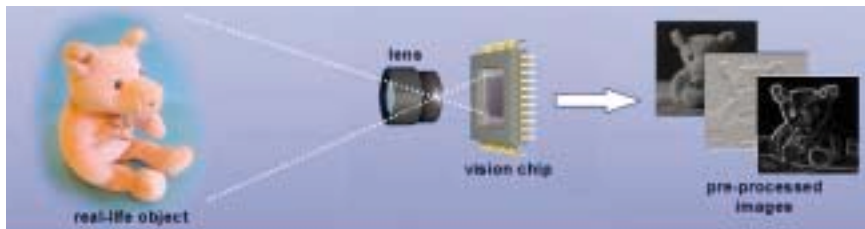
The Scamp-3 is a 1-cm² chip fabricated in 0.35-micron CMOS that arranges its 16,384 pixel-processors in a 128 x 128 array. Each pixel-processor measures 50 microns² and consumes 12 microwatts when running at 1.25 MHz, giving the chip a computational power efficiency of 104 billion instructions per second per watt.

As is often typical of vision chips, the

processors are implemented with analog circuitry. In this case, each analog processor is programmable, so that true single-instruction multiple-data operations can be performed as an image is acquired. Current-mode logic is used throughout the pixel-processor design.

A multiplier, a flag register and six general-purpose registers form the heart of the analog processor. Photodetector circuitry, I/O and four communication registers that address neighboring pixels are also implemented in current-mode logic.

CONTINUED ON PAGE 58



Only a lens and Scamp vision chip are needed to do sophisticated image detail extraction.

Imaging's next wave finds apps

As a graduate engineering student at Stanford University in 1992, Dave Yang began experimenting with CMOS pixel sensor technology. Deciding that imaging capability could be much improved by adding an analog-to-digital converter at each photodetector on-chip, he developed a novel system that can reproduce megapixel-level resolution using only 400,000 detectors per chip. More important, Yang's approach results in a dynamic sensing range 250 times that of standard CCD imagers.

Realizing the potential of his creation, Yang founded Pixim Inc. (Mountain View, Calif.) in 1999 to commercialize the approach. With backing from a number of venture capital firms and TSMC, which manufactures the imaging chips, Yang has tackled the rapidly growing security camera market. Putting A/D converters on every pixel has produced cameras with unusually acute vision.

A key concept behind Yang's design is the ability to monitor and control the collection of photons individually for each photodetector on-chip. The company likens the architecture to an imaging chip in which each pixel operates like an independent camera. The chip's extremely high dynamic range arises from the ability to

turn off pixels that are becoming saturated at high light levels, while allowing detectors that are getting low light to remain on longer during image acquisition.

Other companies are finding niche markets for imaging chips that integrate image processing at the pixel level. Centeye, for example, was founded in Washington in 2000 by Geoffrey Barrows, who developed an imaging chip that senses motion. The company builds custom imagers for clients developing robotic systems. Centeye is also developing Ladybug, an optical flow sensor based on insect's eye architecture.

Neural-net sensors, artificial retinas

NeuriCam Spa (Trento, Italy) has used system-on-chip technology to build image sensors that implement neural-network processing to perform image classification. The company is marketing the technology as a set of intelligent vision chips for products such as smart single-chip cameras; fingerprint, face and iris biometric systems; and security and traffic control.

Entrepreneurs are also tackling the challenging area of artificial retinal implants that could restore sight to the blind. In this case, mimicking the retina is essen-

tial to getting a system that would be compatible with the neural circuitry in the eye. One big challenge is getting a built-in power source and reducing power consumption to the absolute minimum. The problem is heat: A biological system like the eye cannot tolerate heat buildup.

Alan Chow founded Optobionics Corp. (Naperville, Ill.) to develop a solar-powered artificial retina that does not require an external power source. Instead, incident photons provide the power. The company is working on a 5,000-photodiode silicon chip based on the technique.

Elsewhere, a 16-pixel artificial retina developed by Second Sight (Sylmar Calif.), was recently implanted during an experiment at the University of Southern California's Biomimetic Microelectronics Systems Engineering Research Center. Second Sight was founded by veteran entrepreneur Alan Mann.

Although considered a research breakthrough for implantable vision chips, the resulting imaging system is very limited, indicating that much work will have to be done before the technology is made viable for market. Simply achieving a product that is compatible with the body and is not rejected by the immune system is a major hurdle, let alone creating a sophisticated replacement for the retina.

—Chappell Brown

designwin

Engineering Solutions for Customer Challenges

Tangent Technologies' Goal: Get Designs Right the First Time

Tanner EDA's user-friendly platforms hit the mark

With 22 years of engineering experience under his belt, Mark Wadsworth knows one thing that's always true: getting a design right the first time is critical in the highly competitive and time-sensitive imaging chip market. There's no room for errors, delays or band-aid solutions when it comes to earning a design win.

Now that Wadsworth is developing detector-based solutions for customers such as NASA's Jet Propulsion Laboratory, ImagerLabs, Inc. and Photon Dynamics, Inc., his closely-held philosophy couldn't be more relevant.

"It's important to get the design right the first time," said Wadsworth, president of Tangent Technologies, an IC house in Monrovia, Calif. "We are a small company doing highly customized work. We need to make sure we can do the best job from the very beginning."

Wadsworth, a long-time industry veteran who has been a member of the design teams at Texas Instruments and NASA's Jet Propulsion Laboratory (JPL) before launching Tangent three years ago, uses Tanner EDA's HiPer Silicon platform to help on that front.

"I believe we would have never been able to do some of the things we're doing without Tanner," he said, specifically referring to Tanner's easy-to-use features and out-of-the-box capability.

Fitting into Tangent Projects

Tangent is working on key projects that require not only precise imaging designs but quick turn-around, Wadsworth noted.

One major project is developing a charge-coupled device (CCD) that detects charged particles instead of light. These particle detectors will be used in mass spectrometers and other ion detection systems. Such systems are commonly found at airport security terminals to detect explosives. The idea is to provide an IC, built on

an MOS process, that meets the hardware manufacturer's desire to shrink their large system to the size of a laptop, thus providing greater flexibility where the system can be implemented.

Also on Tangent's to-do list is a chip NASA will use in an upcoming trip to Mars. Wadsworth, who worked on an imaging chip for the first Mars Rover expedition while at JPL a few years ago, has another chip on the upcoming Mars Reconnaissance Orbiter mission in 2005, and continues to work with JPL scientists on the development of a chip for a Mars Rover-based RAMAN spectrometer.

Wadsworth, who began using Tanner Tools about nine years ago, credits the design software for the successful implementation of the imaging chip in the first Mars Rover expedition. Getting it right on the first tape out made all the difference, he added.

Wadsworth says he can do everything he needs to do — from layout to verification — with the Tanner platform, and for a small business owner with limited financial and manpower resources, the benefits are enormous.

"We have to be extremely effective on these projects," Wadsworth said. "With most other tools, there's often quite a bit to do when you bring up a design tool. For instance, you usually need someone to do extensive set up and configuration. That's often a full-time job for someone."

"The beauty of Tanner is that it's a self-contained package. It contains everything you need," he added. "You buy it, put it on your computer, and within two hours, you're in business."

The Results

For Wadsworth, using Tanner EDA's HiPer Silicon has produced various other benefits, as well.

One is faster design cycle times. Typically, a design for custom products using Tanner EDA could take two months from initial concept to tape out, Wadsworth said. Without the proper platforms design time can triple, creating a time-to-market gap that would leave Tangent in the competitive dust. The seamlessly integrated Tanner EDA tools also provide Tangent with the ability to easily reuse or modify portions of earlier proven designs. This enables a modular approach to design and layout that greatly shortens the time from concept to first prototypes.

For example, when the manufacturer of the miniatur-

ized mass spectrometer approached Tangent, they requested six different versions of the charge sensing detector in order to test different performance criteria, Wadsworth said. Tangent was able to turn around all six versions within six weeks, he added.

"We were able to do that because of Tanner," he said. "We wouldn't have even bothered to take on that project if we didn't have the right tools to help us."



A-GLANCE:



Tangent Technologies

Headquarters: Monrovia, Calif.

Line of Business: Detector-based solutions for science and industry

Founded: 2002, Privately held company

Key Products: Custom CCDs and imaging ICs for various sectors, include aerospace and industrial markets

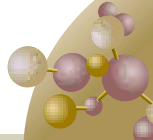
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Vision chips

FROM PAGE 56

All circuit components are connected by an analog bus.

"We plan to use Scamp-3 as the eyes for an intelligent robotic system that can react to its environment and correct itself without human intervention," said Dudek.

In this project, called Reverse-Engineering the Vertebrate Brain (Reverb), the Scamp-3 chip will serve as the eyes for a BAE Systems Plc platform with the goal

of enabling robots to respond to novel events in a manner similar to humans. The Reverb project head, professor Kevin Gurney at the University of Sheffield, will coordinate the efforts of EEs and computational scientists at the University of Sheffield, University of Wales (Aberystwyth), Bristol University, University of Oxford, University of Cambridge, University of Dundee and BAE Systems. The five-year project is funded with about \$3.5 million by the U.K. Engineering and Physical Sciences Research Council, a funding agency for research and training in engi-

neering and the physical sciences.

"Scamp silicon retinas are based on the human eye and work in a similar way to give robots excellent peripheral and central vision," said Dudek. "Like the human eye, our chips process very complex images at rapid rates, thereby filtering the raw data before passing its results along to the robot's brain. We hope this will enable robots to react in real-time."

Unlike a "dumb" video camera that merely records light intensity, the human eye integrates neural networks into each retinal cell, providing real-time informa-

tion processing as photons arrive. As a result, only high-level information, such as edges and motion, are passed up to the brain. Conventional CCD and CMOS pixel sensors can be used to perform the same motion or edge detection, but at the cost of large amounts of digital computation after the images are acquired. By mimicking the retina, vision chips can eliminate most of that added computing equipment.

Currently, researchers with the Reverb project are attempting to blueprint the manner in which the human eye-brain system translates what it sees into control signals that provoke an immediate, effective response by actuators. This model will be used to wire the Scamp "eyes" to the robot's "brain."

"Reverb enables researchers from a number of disciplines and institutions across the U.K. to work together to understand how the human nervous system integrates sensory information to

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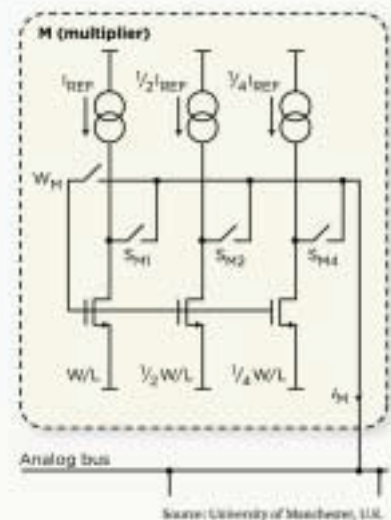
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EETIMES

Vision chip mimics eye
Scamp-3 lets robot see like human



guide behavior," said project leader Gurney. "Hopefully, we can then transfer these insights to the architecture of robotic platforms."

BAE Systems already has plans to utilize the technology in its laser-guided Crawler robot, which can autonomously machine and inspect high-precision aircraft parts.

"Our basic premise is that nature builds systems very well and if we can mimic those systems, then we have a chance to build better robots—ones that combine the best of both the computer and the human worlds," said Dudek.

The third-generation Scamp is the result of seven years of research by Dudek and his colleagues. Reverb currently plans to augment Scamp vision chips with two traditional video cameras: a high-resolution camera for taking "close looks" and a lower-resolution peripheral camera for "keeping an eye out."

The prototypes could be easily scaled using commercially available CMOS fab lines, the team said. Dudek estimated that a 256 x 256-pixel array built with an 0.18-micron process would perform 500 giga instructions per second while dissipating only 2 watts.



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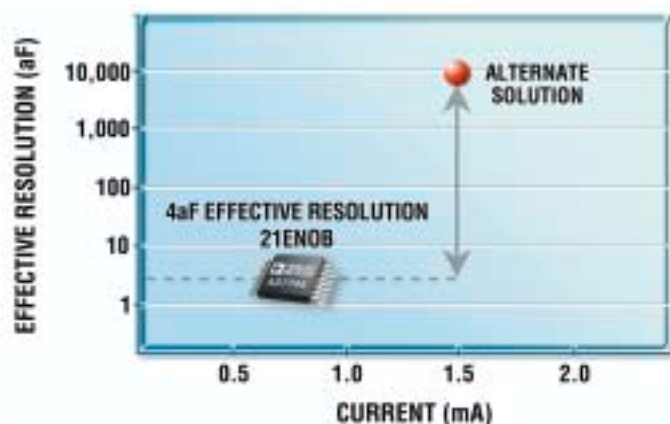
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The road to better yields

Art of Design:
Open hardware opens doors

Tip of the Week:
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Industrial networks move to STANDARDS

Networking has been an important part of capturing and evaluating data from industrial processes. For the most part, industrial networks have been limited in capability, closed in topology and special-purpose in the protocols and data they've carried. Increasingly, however, these solutions are

being supplanted by broader standards, such as Ethernet, running TCP/IP

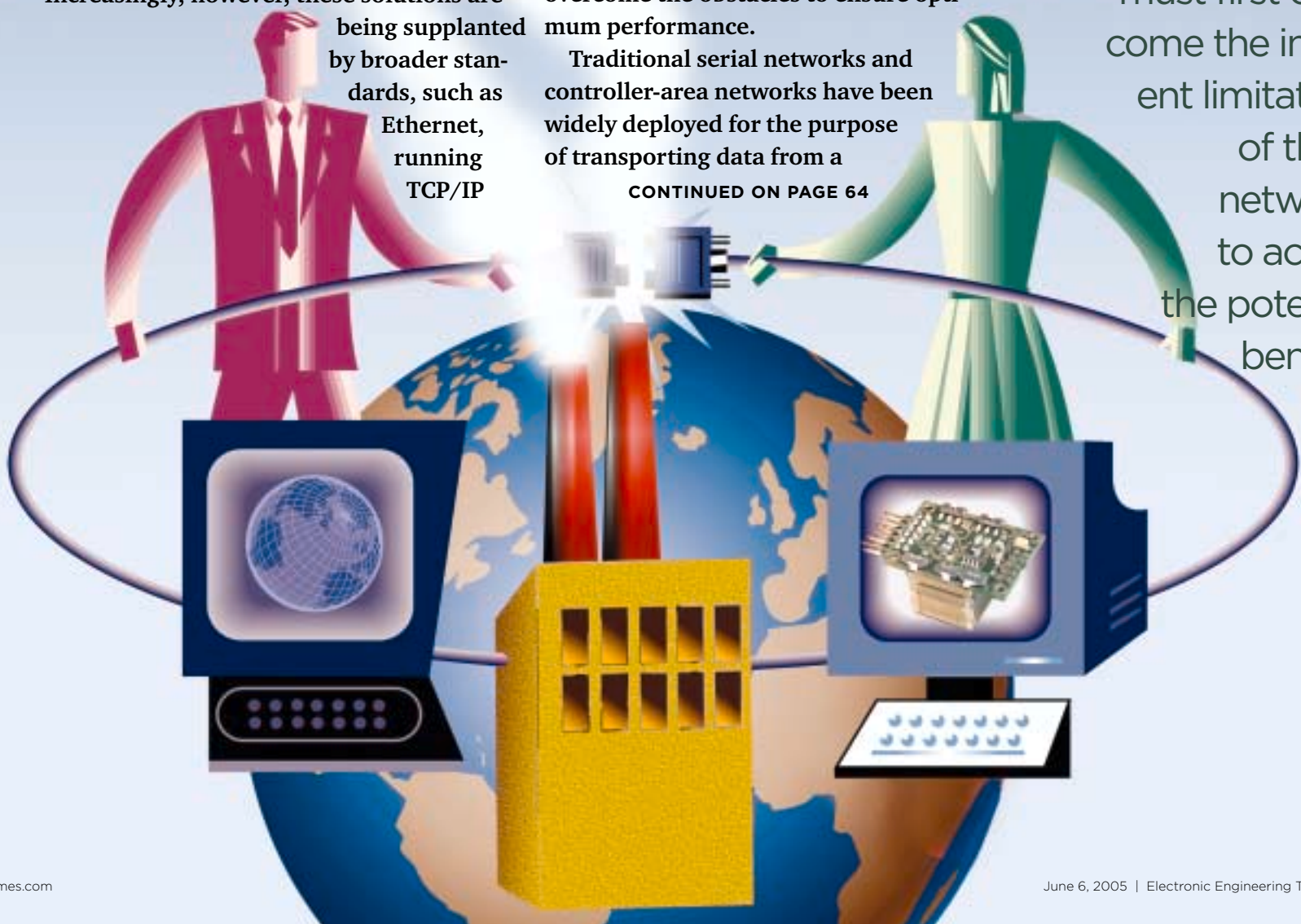
and even Web protocols either in addition to or in place of more-real-time or proprietary interfaces.

The problem with the migration to standardized networks is that those nets were not designed for rugged, real-time environments. Nonetheless, the demand is there, so the onus is on the designer to overcome the obstacles to ensure optimum performance.

Traditional serial networks and controller-area networks have been widely deployed for the purpose of transporting data from a

CONTINUED ON PAGE 64

While standards such as Ethernet enable wider integration, a designer must first overcome the inherent limitations of those networks to accrue the potential benefits



Industrial nets

FROM PAGE 63

device or sensor to a recording instrument or readout. Though still popular, they are being replaced by newer Ethernet, TCP/IP and Web-based networks in a trend that is driven by several factors. Chief among them is the perceived cost benefit of Ethernet as well as the ease with which the TCP/IP protocol stack can be configured and used for a wide variety of transport purposes.

In some cases, end users have bought into the compelling message that it can be possible to deliver real-time process information right to the executive boardroom. The reality, unfortunately, is that while engineers have the technical wherewithal to deliver any amount of data to any location, that ability has to be tempered by some sober realities as to the side-effects of those configurations.

The Ethernet interface was designed to support general-purpose networking, not for the extreme physical conditions of industrial or manufacturing environments. Also, the TCP/IP protocol stack was designed for reliable delivery of static content and does not guarantee the speed or order of packet delivery.

While both hardware interfaces and software protocols are highly flexible, designers need to be cognizant of the limitations of each in an industrial environment and know how to work around them to deliver robust and lasting solutions for process monitoring and control.

As data acquisition devices, programmable-logic controllers, sensors, instruments and other systems on the factory floor grow increasingly dependent upon each other, end users seek broader networks and network applications that can be used in a highly integrated environment. While the thought of office workers monitoring and optimizing factory processes on their PCs between coffee breaks seems absurd, there are a number of applications where the use of a single network standard can pay off.

But designing such a system and building devices that can take advantage of it pose significant engineering challenges. Possibly the most severe constraints on the network are environmental extremes: Manufacturing facilities and industrial sites are often host to high heat, high humidity and electrical interference. Shielding on conventional Ethernet may be able to protect against much of the electrical interference, but hardware reliability and redundancy are also essential ingredients.

One compelling solution is device-integrated networking—that is, enabling Ethernet networking as a part of the silicon,

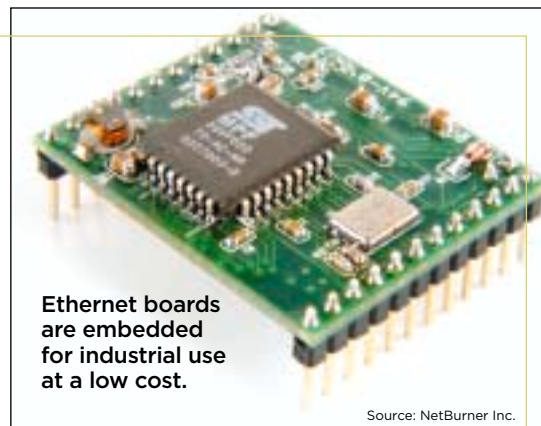
to yield a solution that's both robust and high in performance.

There are several levels at which this integration can occur. Designers can integrate at the chip level, through a custom ASIC or commercial integrated processor such as NetSilicon's NET+ARM. The NET+ARM processors use the ARM7 or ARM9 processor core and integrate 10/100Base-T Ethernet as well as a number of peripheral connections, such as USB and PCI. NetBurner offers a similar configuration with the Motorola ColdFire 5270 microprocessor, flash memory, SDRAM and 10/100 Ethernet.

Integration can also occur at the board level, with standard processors, Ethernet and other peripherals on the board. Boards can typically add more processing capabilities and external interfaces, such as digital I/O, analog-to-digital and D/A conversion, and serial ports supporting

with an alternative that's specifically designed for real-time industrial systems.

Many vendors, including NetBurner and NetSilicon, choose to optimize protocols and interface hardware. Often the user is given the choice of which protocol to use for the data transport, providing the ability to adopt a higher-performance



Ethernet boards are embedded for industrial use at a low cost.

Source: NetBurner Inc.

While this alternative diverges from an Ethernet-only solution, it makes it possible to gain connectivity to Ethernet-based networks in order to achieve transport beyond the factory floor. This approach can provide the best of both worlds—better real-time performance on the industrial side of the network, with data accessibility for monitoring and evaluation on the general-purpose side.

A word about security

Virtually all end users perceive the threat by viruses, worms or system hackers to disrupt or compromise their fundamental business. But as Ethernet and TCP/IP-based solutions become more popular, they open up the industrial network to many of these same hazards.

Viruses, worms or other automated intrusion can obstruct or invade systems running monitoring applications. While it's unlikely such rogue code can affect instruments or devices themselves, it can bring down servers or desktop systems that are often used to monitor and record data.

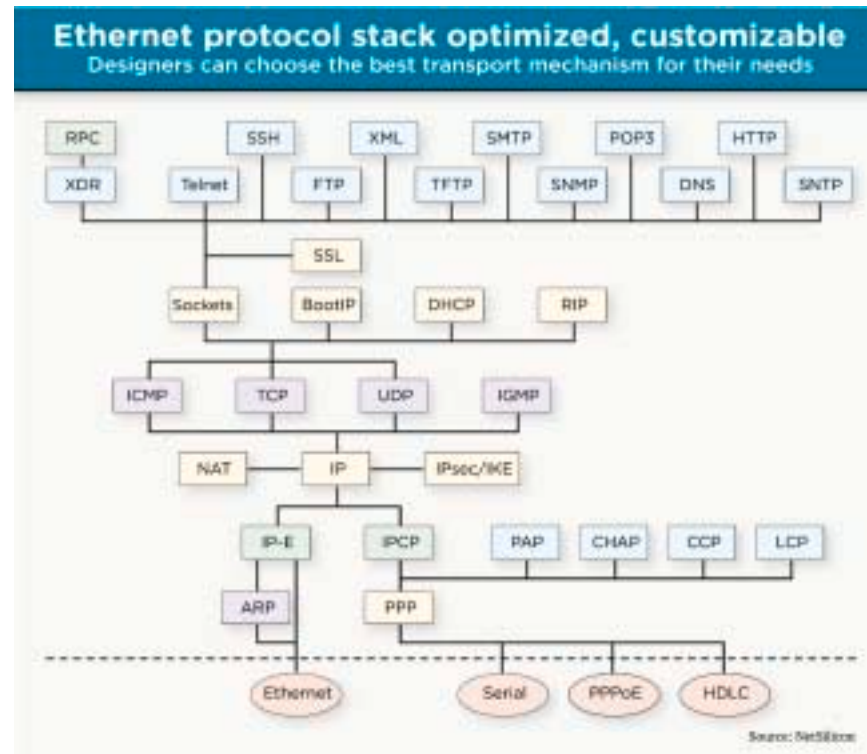
A second hazard is an automated denial-of-service attack, which doesn't affect the network itself but can render the network inaccessible from the Internet. If the software solution includes remote monitoring or control, such an attack would break that link in the chain. Denial-of-service attacks are sometimes intentionally done, either in retaliation or as a blackmail threat.

A final hazard is human intrusion. Such an intrusion is intentionally malicious and can be geared toward either disrupting operations or conducting industrial espionage. Small device networks based on industrial standards offered some level of protection through obfuscation, and from the standpoint of the intruder, there was little to gain. But with broad-based Ethernet networks covering both factory floor and corporate office, the prize has become bigger and the technical challenge within reach.

Another potential threat, still further on the software side, is the increasing use of Linux derivatives as embedded real-time operating systems. While there is nothing inherently insecure about Linux, its increasing use in both computer systems and industrial devices is making it a target for those who understand and exploit weaknesses. Other RTOSes may be safer, if only because they have less exposure to general-purpose use.

How do you design industrial systems to take these and other new security issues into account? Most do this primarily through software, although hardware-based authentication and access are also possible. The software standard for authentication is Kerberos, which is capable of operating on an insecure network. When a user needs to access a network device, first the client requests a ticket for that service from the Kerberos server. The server creates a packet with the content

CONTINUED ON PAGE 80



RS-232 and RS-485/422. Advanced Micro Devices, for example, offers the Net186 Embedded Ethernet reference design, which includes the Am186ES microcontroller, flash memory and synchronous DRAM, serial ports, and a network controller.

At the software level, Ethernet with TCP/IP has some less-than-desirable characteristics as a protocol stack. Specifically, these protocols minimize but don't prevent collisions, and they don't guarantee delivery of packets in order or within a specified time.

There are two approaches to mitigating these protocol issues. The first is to optimize either protocols or hardware within the Ethernet stack to compensate. The other is to use the basic hardware and network approach but replace TCP/IP

protocol or, in general, one that best meets the needs of the application.

Those pursuing the alternative route can use the LonWorks protocol, a layered, packet-based, peer-to-peer communications protocol designed for the requirements of control systems, rather than data-processing systems. Like the related Ethernet and Internet protocols, it is a published standard and adheres to the layered architectural guidelines of the International Standards Organization's Open Systems Interconnect reference model. The LonWorks protocol works to eliminate packet collisions, which are the primary cause of performance degradation. Connectivity to Ethernet, the Internet or a wide-area backbone network is possible through the use of LonWorks-to-IP routers.

By Peter Varhol
(peter@petervarhol.com),
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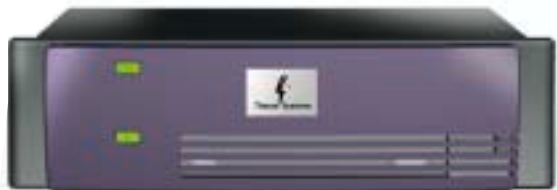
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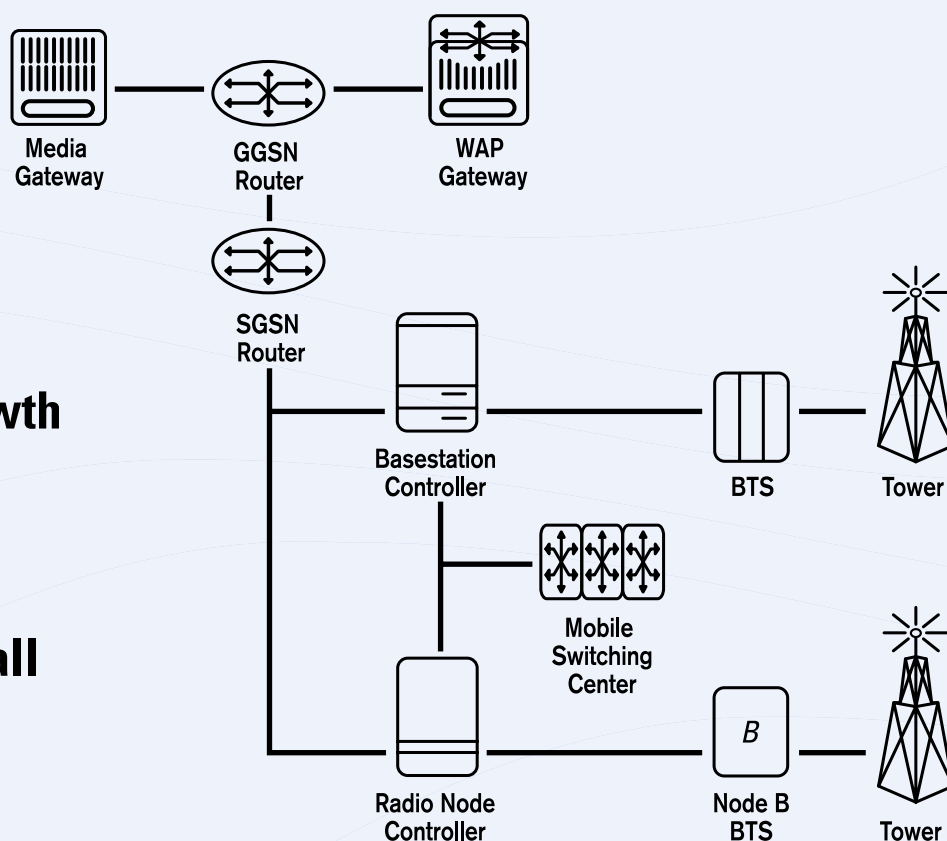


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Choosing wisely for ZigBee apps

The ZigBee low-power, low-cost wireless-networking standard is making it practical to embed wireless communications into everyday appliances. Its proponents say the standard will foster rich new markets for home and building automation, energy conservation and even homeland security.

While the ZigBee v1.0 specification has finally been ratified, the protocol isn't a one-size-fits-all blueprint for companies wishing to tap into this market. At its most basic level, ZigBee ensures interoperability with other standard-compliant products. The deeper application, architectural and platform issues that developers must weigh are as wide-ranging as the potential applications themselves.

The ZigBee standard provides network, security and application support services operating on top of the IEEE 802.15.4 media-access control (MAC) and physical-layer wireless standard. It

By Zachary Smith
(zachary@ember.com), chief software architect for Ember Corp. (Boston)



employs a suite of technologies to enable scalable, self-organizing, self-healing networks that can manage various data traffic patterns.

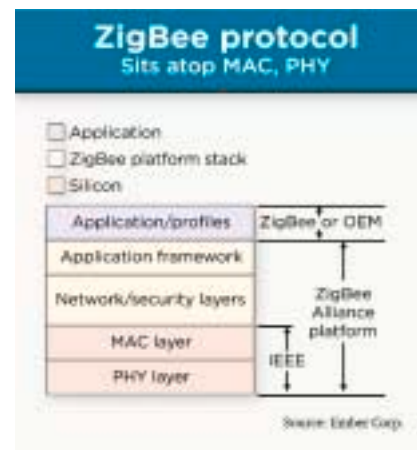
While ZigBee is often thought of as synonymous with wireless-mesh networking architectures, the standard actually supports several network topologies, including star, cluster tree or star/mesh hybrid networks. Consequently, the first consideration a developer should address is which network config-

uration best suits its application requirements.

If data reliability is key, mesh network architectures offer the best protection against the inherent vagaries that cause signal degradation in any wireless environment, such as RF attenuation, electromagnetic interference and multipath signals. Placing ZigBee receivers and transmitters closer together mitigates the destructive effects of all three conditions. And the redundant paths of mesh networks ensure alternate data paths and no single point of failure.

Other applications may require ZigBee routers to extend the network's range by acting as relays for nodes that are too far apart to communicate directly. Moreover, the deployment may rely on battery-powered routers that need a significant amount of "sleep" time to increase their lifetimes.

Consider a crop-monitoring network or similar agricultural application. Here, a cluster tree configuration would work best. It can aggregate multiple subnetworks into a long-distance ZigBee wide-area network in which low-data-rate traffic trickles along the tree, awakening



the battery-powered routers only when needed to send or receive data between the appropriate subnets. Conversely, some shorter-range applications may be better suited to a star topology, where the communications overhead of mesh network routing may not be necessary.

Easy interoperability

While ZigBee is an open standard, it also grants OEMs great latitude in how much of their product should be open to third-

FROM INTRODUCTION



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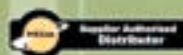
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party vendors. Because the ZigBee standard defines only the network, security and application interface layers, developers can license the entire ZigBee stack, which can include application profiles for a specific product, or merely license the networking layer for basic network-level interoperability.

At the application layer, developers must decide whether to use a public application profile or develop their own private profile. ZigBee v1.0 has already defined basic public profiles for lighting, with application profiles for HVAC, industrial sensors and other sensors in the pipeline. Any company may design products compatible with products sporting public profiles.

For example, a fluorescent-lighting ballast vendor using the public ZigBee lighting profile can interoperate with third-party light switch dimmers using the same profile.

Developers can add their own look and feel to the public profile. ZigBee devices are modeled using application objects, which communicate with other devices by exchanging the profile objects and their attributes.

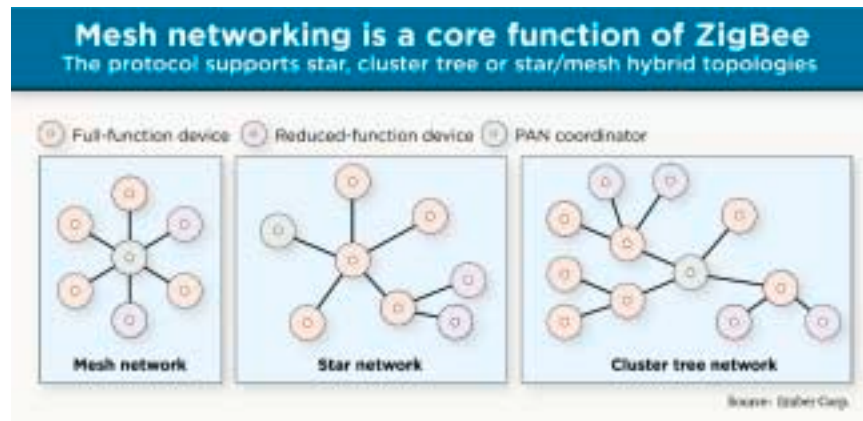
While it might seem contradictory to

ZigBee's spirit of openness, some OEMs may develop products that don't provide open interoperability at the application layer. Developers can design private application profiles to create a closed "ecosystem" of single-vendor devices, or they can select third-party devices. ZigBee defines an abstract interface, while platform vendors provide application programming interfaces that define rules for how applications integrate into the ZigBee stack.

A "closed" system still benefits from third-party product manufacturers at the network level. Required interoperability at ZigBee's lower stack provides data routing as well as media-access control, network formation and maintenance, and device and service discovery.

How that data is transported is another key concern for developers, because ZigBee doesn't define a transport layer.

Developers must decide whether to build the transport mechanism themselves or to design their applications using a ZigBee chip that has a built-in transport layer. For example, Ember provides a transport layer with its ZigBee stack as a way to simplify application development and ensure reliable



end-to-end messaging. The transport layer provides the framework on which developers define private ZigBee profiles.

Security concerns

Most ZigBee solutions will require some level of security. Toward that end, ZigBee provides a standardized tool box of security specs and software, based on a 128-bit AES algorithm, and incorporates the security elements of 802.15.4. ZigBee stack profiles define security for the MAC, network and application layers. Security services include methods for key establishment and transport, device management and frame protection.

If developers choose to use a public ZigBee profile, then the security decisions for their applications have already been made for them; they're predefined in the profile. Chances are that even if a developer intends to build a private-profile application, he'll choose the security mode in one of ZigBee's predefined stack profiles.

At this level, developers must decide issues such as whether they need to encrypt the data frame's payload, as well as the length of the authentication code (8, 16 or 64 bit, and so on) tagged onto the end of the frame. Basic applications may not require authentication and thus can

CONTINUED ON PAGE 80

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Will next iPod be a phone?

Everybody agrees that MP3 technology is going to stay around for a while due to its success and growth. The question is, in what form factor? Will it remain an independent device, generating millions of dollars for Apple and other OEMs? Or will cellular phones swallow the MP3 functionality in the same way they swallowed the "just for fun"-use digital camera, leaving little room for standalone MP3 players? Other than the business consequences for the MP3 manufacturers, what are the technical hurdles?

In March, the CTIA Wireless conference tried to clarify the road map of where the cellular market is going. It was clear that next year cell phones will try to do even more than they do today, including delivering music. Consequently, and as early as 2006, the independent MP3 device manufacturers (led today by Apple) might be forced to think differently.

The MP3 integration argument centers on three issues: power consumption (and its counterpart, battery size); overall form factor; and the fact that MP3 players, and Apple iPods specifically, are a marketing phenomenon. People love their iPods too much to replace them with phones. This leads to eager anticipation about Apple's co-development in cell phones.

Several phones already support MP3

By Cedric Paillard
(cedricp@semiconductor.com), *TECHinsights*
director at Semiconductor Insights (Kanata,
Ontario; www.semiconductor.com)



playback capabilities, including the Motorola MPx 200, Nokia 6630 and Siemens Sx1. Still, an MP3-capable cell phone is limited in the number of songs that can be stored. However, specific alliances between handset manufacturers and MP3 vendors may address that issue. Motorola has joined with Apple and Nokia is working with LoudEye, while Microsoft MSN Music has teamed up with Qualcomm. These coalitions will help the transition to new cell phones with a focus on digital audio playback.

Technical hurdles

Three technologies will have to be further developed to move MP3 capabilities into a cellular phone. First, storage capacity needs to be increased—within a smaller form factor. There is currently a trade-off between using flash memory technology and micro drives. Flash memory devices are inexpensive, small and consume little power. However, they are limited in storage capacity. Although 1-Gbyte devices are now readily available, this is still not enough for mass-

data storage. Micro drives are great for mass storage, capable of exceeding 40 Gbytes. But the power consumption and size are relatively high compared to the rest of the mobile phone. Drives are also made from fragile moving components. That said, the Samsung SPH V5400 includes a micro drive with a 1.5-Gbyte capacity.

Power consumption, as mentioned above, is a strong limiting factor for converged devices. A third technology that must be further developed is music content downloading via service providers. This would allow customers to access songs without having to be connected to a computer. It would require a cheap, fast solution. To this end, HSDPA, EV-DO and other technologies either are being designed now or are in trials.

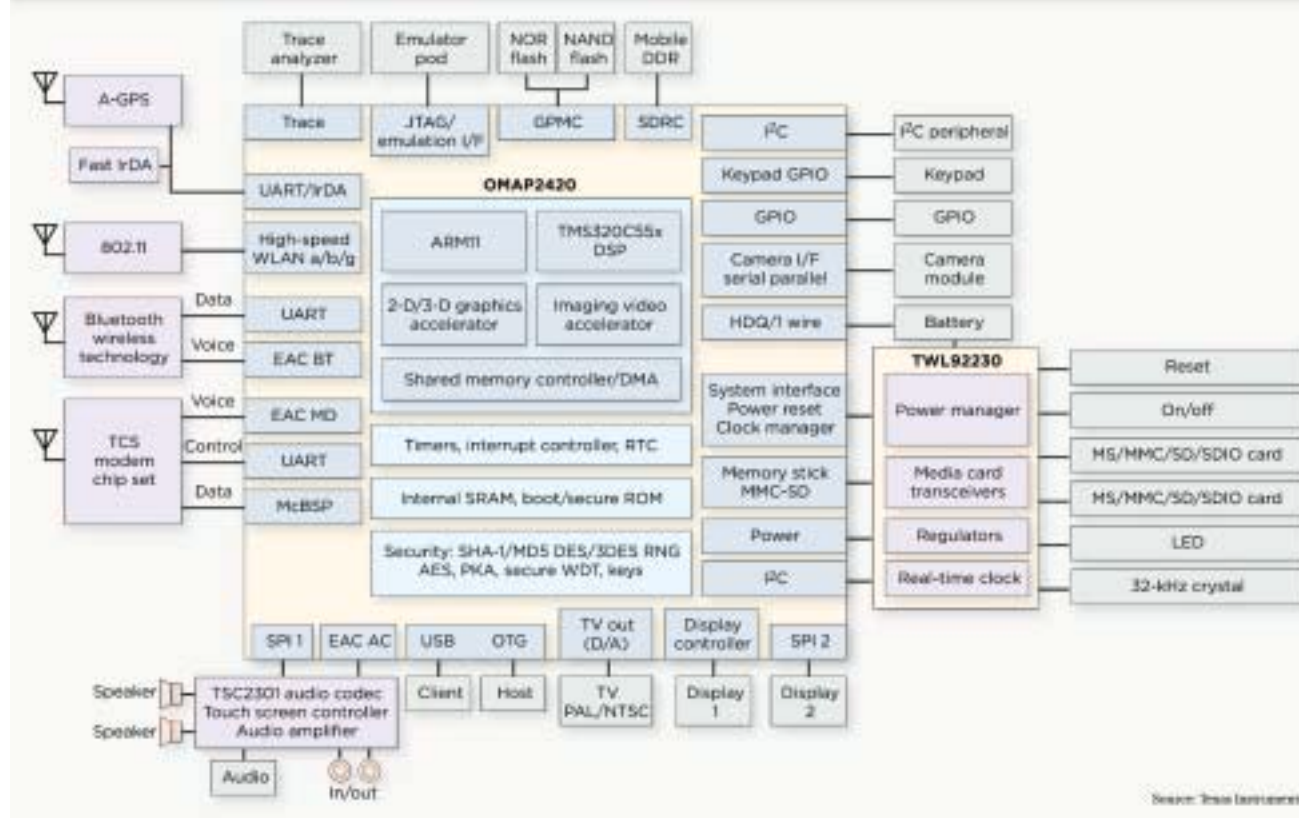
Application processors provide one way for OEMs to reduce the overall bill of materials (BOM) and the power consumption of the system. Such devices from companies like Texas Instruments or Qualcomm are different from those of an MP3 encoder/decoder such as that offered by SigmaTel. Both types are highly focused; but the difference in usage models is pushing implementation of a different set of features to efficiently support the application, with a significant impact on power consumption.

Solutions providers are developing advanced power-saving strategies that involve both hardware and software intellectual property. The differences ride on which functionality is integrated on the

CONTINUED ON PAGE 72

TI's Omap 2420 apps processor uses external power control

Approach makes sense since cell phones are more complex than MP3 players



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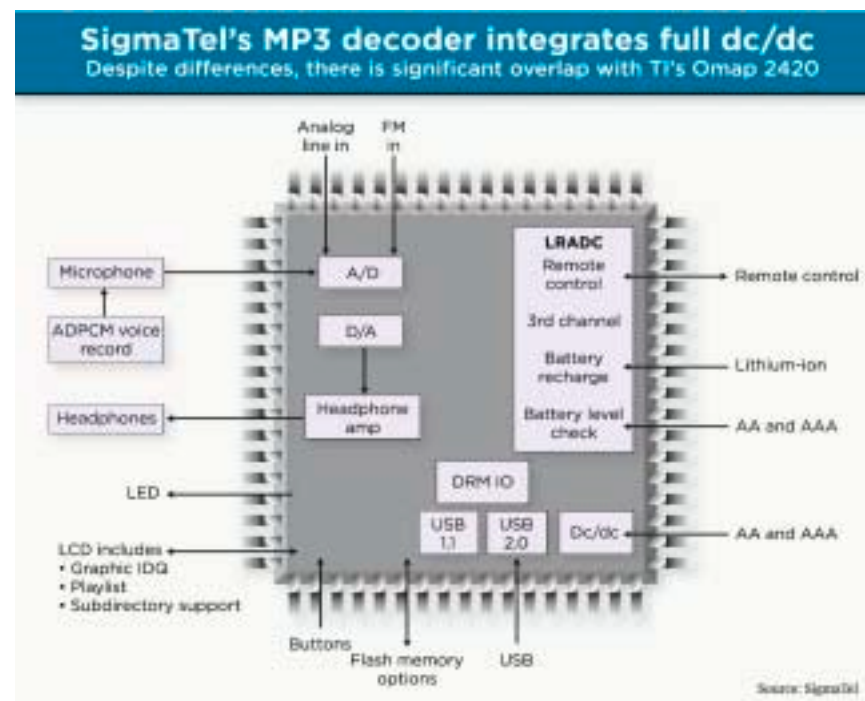
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MP3 phone

FROM PAGE 71

die, so let's compare two leading architectures: the SigmaTel MP3 decoder and the TI Omap2420 application processor family. SigmaTel elected to integrate a full dc/dc converter on-chip, thereby reducing the overall BOM of an MP3 system. This is an interesting approach and not an easy one, considering that the same device also integrates all the audio codec functionality on board. On the other hand, TI's Omap2420 relies on an external power-management chip. This approach makes sense, since a cellular phone is a more complex product than an MP3 player, having additional features that require more stringent power control.

At first glance, it seems as if the Omap2420 or a Qualcomm MSM65xx processor would be able to do the job of the SigmaTel STMP3520B, requiring only minor changes and reuse of their powerful, integrated DSPs. In practice they would be able to accomplish this, but the application specifications carry a cost not associated with the final application. For example, the SigmaTel IC is designed to support a large set of flash memory, whereas the TI or Qualcomm parts would support a more reduced set of storage solutions. SigmaTel



also supports more audio interfaces. TI and Qualcomm don't have to; there is not enough demand to justify the integration of those features in a handset.

Application processors carry DSPs dedicated to specific mobile-phone-type applications not required in an MP3 play-

er. It is also important to note the common set of features in all the entries, such as the LCD controllers, USB interfaces, and serial and parallel interfaces.

This quick comparison highlights an even more important trend. It is not only MP3 music applications that are going to

be swallowed by that handset, it is the entire multimedia platform, including video. Due to the power consumption issues, it is unlikely we will see all of those applications working concurrently. But independently enabled, they might lead to new types of cellular phone products, including video and gaming, this year.

Who can best integrate MP3?

The overlap raises questions about who is in the best position to integrate MP3 functionality in a cellular phone from an application controller point of view. TI, Qualcomm and SigmaTel know their customers' requirements very well. The real issue is to understand the user model. Do consumers want a cellular phone with MP3 capabilities or an MP3 player with cellular phone capabilities?

TI recently announced a single-chip GSM/GPRS solution to leverage low-cost mobile-phone solutions. MP3 player manufacturers may see this and similar devices as an opportunity to develop their own MP3 phones. This would resolve a lot of other issues with regard to digital rights management (DRM) and audio quality, areas in which the MP3 player manufacturers have solutions and expertise. Synchronization and ease of use will also be major contributors, while DRM will unlock the portable media market.

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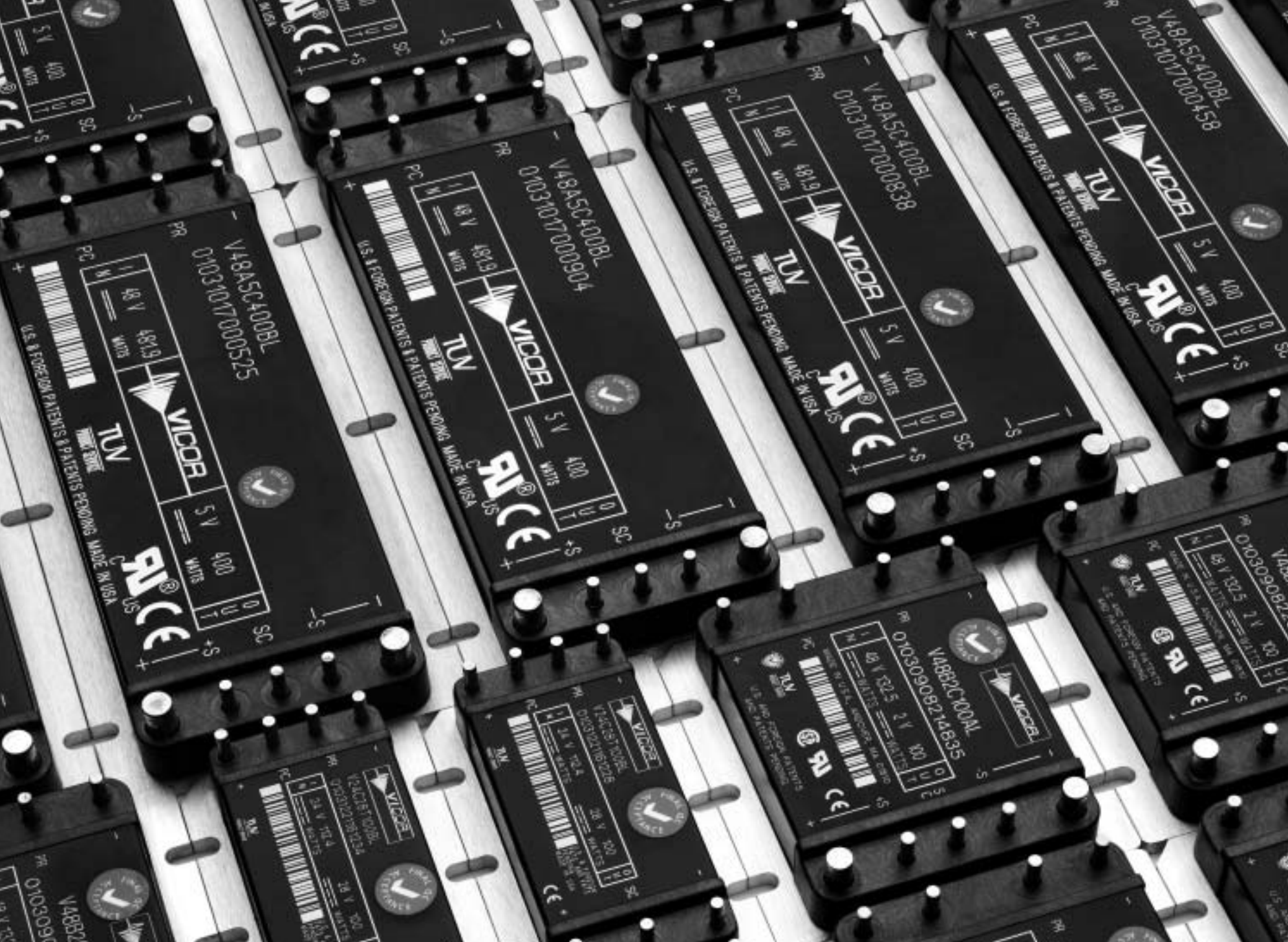
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Think models, not rules, for better yields

As leading-edge companies move to 90-nanometer and smaller process geometries, they are finding that strict adherence to the available design rules is insufficient for high-yield manufacturing. Anecdotes from companies working in the latest processes suggest a chaotic situation, where new rules are being added to the technology files on a weekly basis. Some of the design rules, which are often ad hoc responses to manufacturing problems, are incompatible or mutually exclusive with other rules or with generally accepted practices. For example, the need for multiple vias on minimum-width lines can conflict with minimum spacing for features near those vias.

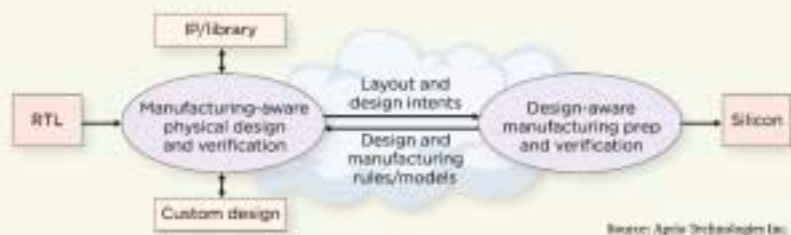
The number and complexity of transformations from design to optimization, implementation, mask and, finally, wafers has created a series of discrete data environments that are not able to share vital information. This situation will lead to a disaster if coordination between design and manufacturing doesn't improve.

Rather than trying to patch the process by adding ever more rules, the industry must change from a rule-based handoff procedure to a model-based, integrated design-to-manufacturing methodology. Designers will have to develop a greater understanding of all manufacturing constraints, while the fabs will need to deliver accurate process and device characteristics. The much-abbreviated list of design process and methodology changes at right starts the path to model-based design and higher yields—and will help stave off catastrophe. For additional information on design-for-manufacturability and the transition from design to mask, check the DFM section at www.SI2.org or see us at www.aprio.com.

By Clive Wu (clive@aprio.com), chief technology officer and founder of Aprio Technologies Inc. (Santa Clara, Calif.)



- **Correct by design, don't design by correction.**
- **Use design tools that incorporate both static (rule-based) and dynamic (model-based) manufacturing effects.** Use static effects (such as design rules) to ensure worst-case performance under known conditions; use dynamic effects to design and optimize for lithography and process corner cases that cannot be easily characterized, and to handle many instances where rules are simply mutually exclusive.
- **Perform more than just the design rule checks for manufacturability verifications.** The design rules are not meant to cover both process and lithography variations; they really are focused on known (fixed) manufacturing issues.
- **Validate statistical models from the fab.** Look over the statistical process control (SPC) reports for your process to confirm mean, variance and distribution of target parameters. Use test results to correlate models and data.
- **Share design intent and content with the fab.** Let the fab know important design information such as critical areas/paths, design specifications and design intent, so it can help to match process and lithography requirements to the design requirements.
- **Insist that your fab share its manufacturing-process information and models.** A lack of processing information leads to open-ended designs and lower yields. A model-based design process needs the process models to close the design loop.
- **Use and reuse manufacturing-proven intellectual property and associated, hardened manufacturing characterizations/modifications (e.g., resolution enhancements).** If you know that some modifications have been implemented on prior silicon and improved yield, use them again.



A true DFM solution builds on the exchange of information between design and manufacturing, and requires tools to share common, open data models.

- **Assume that (mask) manufacturing can correct or fix all layout errors.** The phase shift for one feature may be the opposite of what's required for the adjacent feature, so neither can be optimized. Other reticle enhancements may have similar problems.
- **Use unproven (nonhardened) IP.** Any IP that hasn't been checked for proper function in silicon is suspect and requires extensive DFM analysis prior to use.
- **Try to write the masks without lithography and process corner analysis.** The device variations attributed to processing are less than half of those possible. Lithography variations contribute as many variables as processing, and the full analysis requires a matrix of the effects from both.
- **Support proprietary formats required for data exchange.** The difficulty of working with discrete silos of data is exacerbated by the need to translate incompatible file formats across applications. Open formats and standards facilitate data exchange.
- **Use known low-yielding intellectual property.** If you already know the areas within the IP that have manufacturing problems, fix those problems before using the IP.
- **Use irregular structures and patterns.** The resolution enhancement processes, such as optical proximity corrections (OPC), work best on uniform, balanced structures.
- **Assume the drawn layout is equivalent to the silicon image.** Also, don't assume the statistical average of manufacturing variations represents their nominal values. Systematic process distortions (such as those introduced by OPC) can skew parameter distributions, making the nominal values significantly different from the average.
- **Assume estimates from statistical models are necessarily more accurate.** Vendor-collected SPC data is not correlated to your specific design. Get and use the actual mean and variance numbers that correlate to your design and your process run for best accuracy.

Art of Design

Doors 'open' to hardware

Is "open" hardware a disruptive technology that will foster the kind of collaboration that Linux brought to the software world?

Despite the recent demise of one prominent open-source programmable-logic effort, advocates think so. Given the increasingly prohibitive costs of developing hardware from scratch, open hardware is an attractive possibility. But the road is not easy, and new business models will be needed to support it.

At the Electronic Design Processes workshop last month, Juan-Antonio Carballo, partner in IBM's venture capital group, made an eloquent pitch for open hardware. "The open-source model is quickly extending from software to hardware, and it will provide a similar swell of collaborative innovation," he said.

The word "open" has various meanings, Carballo explained. It includes but is not limited to open source, where specifications or source code are freely available and can be modified by a community of users. It could also mean that the hardware details can be viewed, but not modified. And it does not necessarily mean that open hardware, or designs that contain it, are free of charge.

The open-hardware movement suffered a blow in late April when STMicroelectronics pulled the plug on its Generalized Open Source Programmable Logic initiative. That effort was launched last year in India, with the stated goal of becoming the "Linux of the semiconductor world." While never fully opened to the public, it was seeking "qualified contributors" who would have access to EDA source code and to hardware and software intellectual property (IP).

Still, there are other open-hardware efforts. One (www.power.org) represents a community of developers, tool providers and manufacturers who are developing standards and applications around IBM's Power Architecture. The Power.org mission statement calls for an "open-standard hardware development platform for the electronics industry," with open standards, specifications, guidelines and best practices.

An active community is developing around open-source IP cores. The

CONTINUED ON PAGE 76

The Art of Design offers perspectives on the techniques and business of electronics design. Ideas may be sent to rgoering@cmp.com.



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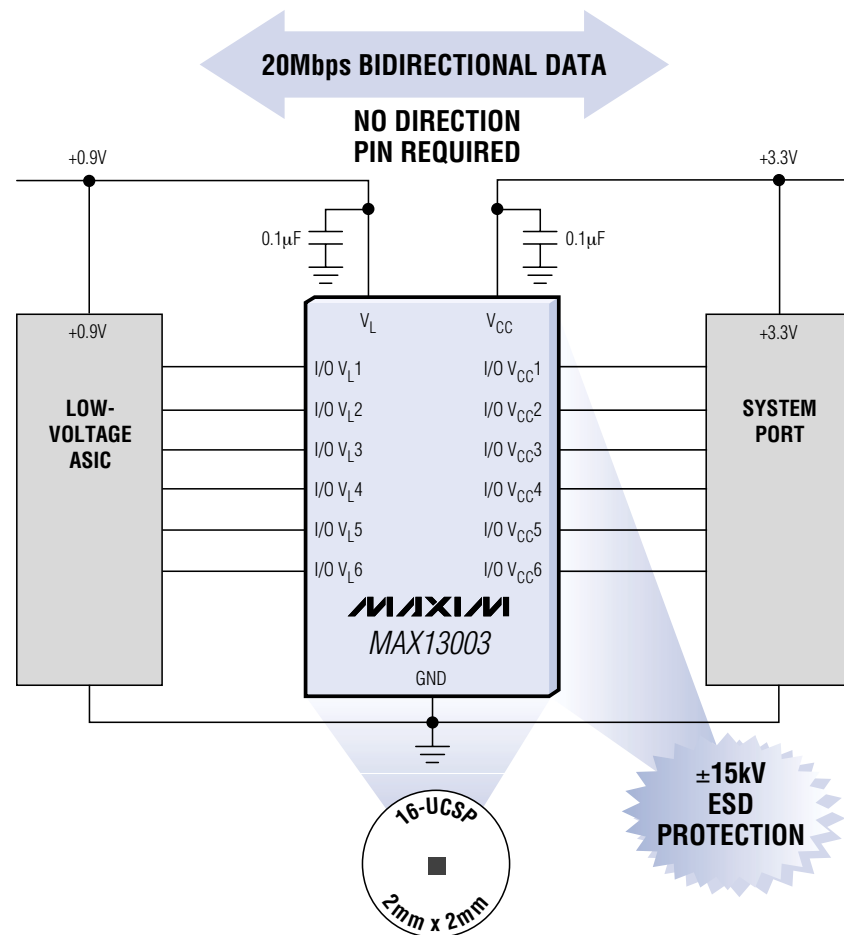
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Art of design

FROM PAGE 74

www.opencores.org Web site lists a number of projects, including cores for arithmetic functions, DSP, communications protocols, memory and microprocessors. An OpenTech CD-ROM compiles several hundred open-source EDA software programs and hardware designs.

One pointed question is how to make money from open hardware. The answer may be similar to that in the Linux world: support and value-added services. At the Opencores site, OpenTech creator Jamil Khatib recently launched OpenSupport, a partner program designed to provide commercial support for open-source designs.

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How instrumentation amps measure up

While their versatility, wide operating temperature range and low cost make thermocouples attractive options for measuring temperature, their low output voltage and use in remote locations often complicate temperature measurements. By understanding typical measurement pitfalls, engineers can make better choices when selecting instrumentation amplifiers for thermocouple designs.

The temperature of the thermocouple is determined by measuring the voltage generated by the junction of two dissimilar metals. This is called the Seebeck voltage, and it changes by 40 microvolts/°C for a Type-K thermocouple. These small input signals can be lost if they are on the same order as the offset and gain errors of the instrumentation amplifier (in-amp). It is difficult to calibrate offset and gain over temperature, so the in-amp must have low offset drift and low gain drift.

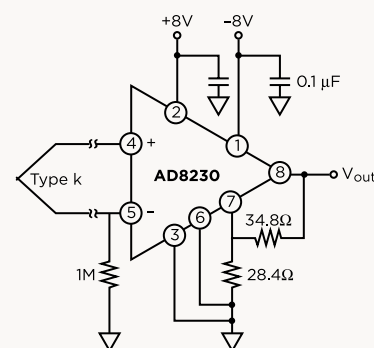
To illustrate the importance of low offset drift, consider a case where a Type-K thermocouple is used to measure the temperature gradient in an oil reservoir. For an amplifier with an 8-uV/°C offset drift specification, a 20°C change in ambient temperature would cause a 4°C measurement error. Unfortunately, the offset drift cannot be separated from the signal.

"Zero drift" instrumentation amplifiers use autozeroing or chopping to minimize offset drift, making them ideal for thermocouple measurements. Leading-edge devices now offer ultralow offsets of 10 µV and offset drift of 50 nanovolts/°C. This drift is three orders of magnitude lower than the 51 µV/°C Seebeck voltage generated by a Type-J thermocouple.

Unfortunately, gain drift is indistinguishable from the signal; it can be particularly insidious because gains of 200 or more are often used for thermocouple measurements. The gain-setting method deter-

mines how tightly gain drift can be controlled.

Amplifier gains are typically set in one of three ways: with matched internal resistors, matched external resistors or a single external resistor setting a ratio with one or more internal resistors. The gain drift of the latter method will be the highest, as the temperature coefficient of the external resistor cannot be matched to that of the internal resistors. Amplifiers that program gain by selecting internal resistors or those that allow users to supply their own



Using matched gain-setting resistors minimizes gain-drift errors.

Source: Analog Devices Inc.

external, matched resistors have much lower gain drift. Thus, gain drift can be minimized by selecting an instrumentation amplifier whose gain is set using matched resistors.

Common-mode voltage is an often neglected consideration. The subject being measured may be located several meters away from the instrumentation. Unfortunately, long thermocouple wires pick up undesirable signals. The mutual inductance from motor coils, for example, can generate common-mode voltages as large as 5 V on a thermocouple. The instrumentation amplifier must be able to accommodate these large common-mode input voltage swings.

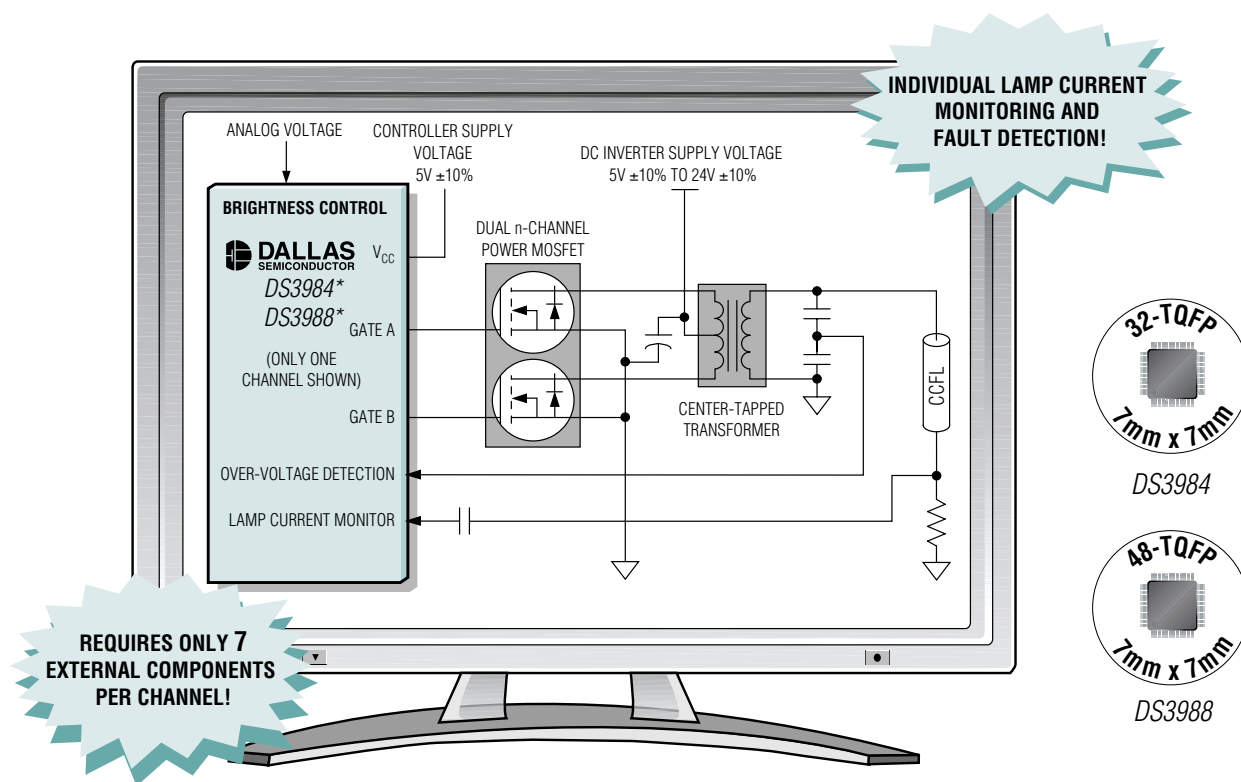
While it is simple to calibrate system errors at one temperature, it is difficult to do so over a product's entire temperature range. Offset drift and gain drift can be particular nuisances. And common-mode voltage should not be overlooked. When selecting an instrumentation amp for thermocouple applications, pick one that addresses these classic pitfalls.

By Stephen Lee
(stephen-p.lee@analog.com), applications engineer at Analog Devices Inc.
(Wilmington, Mass.)



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New growth for EDA's in-house tools

Recent studies and trends project sub-10-percent growth for EDA in the coming years. Two anticipated technology trends boosting this growth have been the tooling necessary to move to 65- and 45-nanometer geometries, as well as the emergence of the intellectual-property (IP) business. But the former depends on the supply-side capability of EDA vendors to roll out these tools in time, and that has proven to be risky for some in that they're competing with their own customers.

However, a third important growth segment—namely, the in-house EDA tool development—bears watching. While on the surface this might seem a

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for SoftJin Infotech
Private Ltd. (Bangalore, India, with a U.S. branch in Santa Clara, Calif.)



revenue loss for the EDA vendors, further analysis shows quite the opposite.

Over the last 10 years, vertically integrated semiconductor companies with large in-house EDA teams have given way to independent EDA companies offering full tool suites. But conditions now developing are leading to a reversal of this trend. Some key drivers: Design-for-manufacture/design-for-yield problems have forced design and manufacturing teams—and fabs—to interact more closely. Companies that have both teams in-house have seen significant IP value in bridging that gap and in having the data stay within the company firewalls.

Leading semiconductor companies have always experimented with new process technologies to differentiate their offerings from the competition. A case in point is 3-D semiconductor technology, which has required a complete overhaul of the physical-design tools. Commercial EDA vendors have traditionally waited for markets to be established before entering

them, leaving startups without access to fab, manufacturing and design data. The semiconductor companies would need to develop these tools in-house.

Programmable platforms (including several by venture-capital-backed start-

Vendors need to change their one-size-fits-all product model.

ups) have emerged recently in such areas as structured ASICs, via-programmable ASICs and single- and multicore embedded processors with programmable data paths. One common thread among all of them: They devote precious resources to developing custom tool chains, since off-the-shelf solutions do not fit their needs.

To tap into this in-house tool segment, EDA vendors need to change their

current one-size-fits-all product model and move toward a more-customized tool-development model. This would involve productizing key reusable EDA technology modules or components rather than the whole tool itself. The reuse of these EDA building blocks will help reduce the overall cost of development and time-to-deployment of such customized EDA tools. The customized portion could be undertaken as a service engagement or the customer might choose to do it. Depending upon the IP risk context, the customer may allow the EDA vendor to productize the customized tool for commercial use and share the benefits. Or the customer might choose to retain exclusive rights on the customized portion and protect a competitive advantage.

A recent survey by Dataquest shows that that number of designers using in-house tools has increased threefold in the last seven years. In-house tools budgets went up 9 to 12 percent in 2004 alone, and *Electronics Business* estimated this market to be close to a billion dollars. Not a bad place to be!

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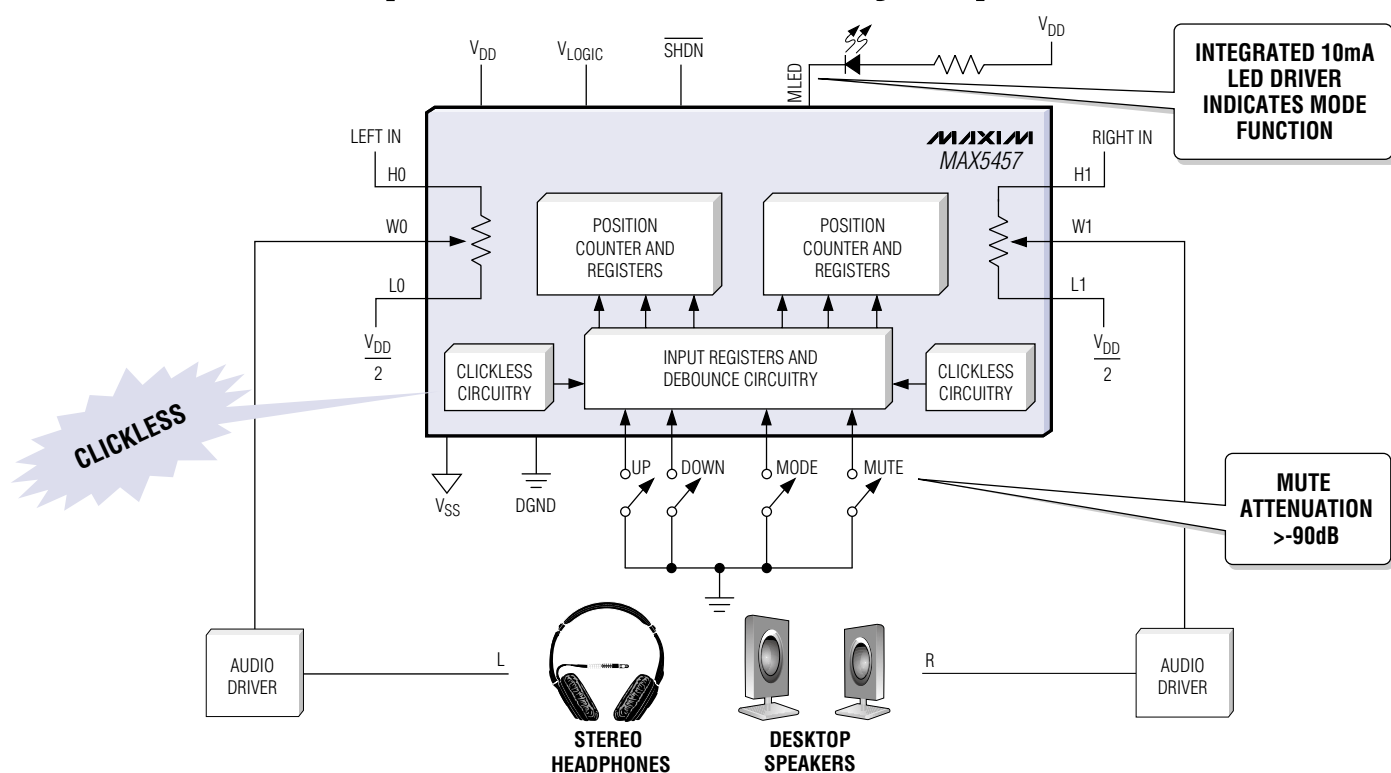
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ZigBee options

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benefit from a smaller packet payload. These data integrity options let developers make trade-offs between message protection and overhead.

Developers must also decide where to apply security: at the MAC, network or application layers. If the application needs the strongest security possible, secure it at the application layer. Security implemented here uses a session key that can be authenticated and decrypted only by another device possessing the key. This approach protects against both internal and external attacks, but it requires more memory to implement.

Security at the MAC and network layers serves essentially the same purpose: to secure single-hop transmissions. The MAC layer inherently mediates access to the shared medium and controls single-hop transmissions between neighboring devices. The ZigBee Alliance added a network-layer security option to add functionality not available at the MAC layer, including the ability to reject data frames if their freshness can't be verified. Both security layers use a global key that all ZigBee devices on the network share.

MAC and network-layer security suit applications that need protection against specific infrastructure attacks, such as a nefarious device maliciously inserted into the network. If a developer needs to establish a route between two devices and the network layer frames aren't secure,

that device could intercept the packets.

ZigBee security also introduces the concept of a "trust center," which lets devices into the network, distributes keys and enables end-to-end security between devices. Here, developers must choose between two trust center modes based on their application: residential or commercial. Residential mode is lightweight, but it doesn't establish keys or

Developers must choose between two 'trust center' modes.

scale with the size of the network. Commercial mode establishes and maintains keys and scales well, but at the cost of significantly more memory.

Platform considerations

ZigBee provides a standardized network and application framework upon which developers can build applications without worrying about the intricacies of networking and RF issues. Yet, by itself, ZigBee's standardized framework doesn't ensure easy product development.

The market is flush with a diverse vendor mix of components needed to build ZigBee-compatible applications, including RF transceivers, microcontrollers, flash ROM, vendor-specific protocol stacks and application development tools. Consequently, developers must choose between rolling their own ZigBee solution

from multivendor components or building their applications on an integrated hardware/software platform. Lacking both the expertise and inclination to tackle the tough integration effort, most developers will probably opt for the latter approach.

The first decision they must make is at the chip and networking-software levels. The biggest challenges stem from the complexities and incompatibilities between hardware and network software. Problems found in development of a new application are rarely confined to just one stack layer. For example, a bug found in the MAC layer of a prototype can rarely be detected and debugged by network-layer providers. Hence, developers must carefully consider the integration depth of their chosen platform.

A ZigBee solution requires an RF transceiver, a microcontroller or DSP for application processing, and a ZigBee network stack. Until recently, most were multichip, multisolution solutions born of multivendor partnerships. Today, a new generation of fully integrated, single-vendor platforms is hitting the market.

Multivendor platforms sometimes offer lower upfront costs. But a single-source platform, while often more expensive, lets developers avoid the headaches and product development delays inherent in solutions built from different vendors' hardware and software products.

Developers must also consider the depth of the networking stack. Typically, the deeper the stack, the easier the development effort. A stack that provides everything from the physical network layer through the transport layer and all the way up to ZigBee profiles will shield developers from the inner workings of the network, freeing them to focus on application development. For example, a ZigBee application built with a mixed-vendor solution would require developers to factor in how their application would handle dropped network packets between nodes. But such complexity would already be accounted for in a single-source, full-stack platform. Tool choices can also make or break a ZigBee development effort.

Consequently, developers must carefully consider both the breadth and the functionality of their platform's development environment. It's important that the vendor provide a full development kit complete with multinode wireless semiconductors, networking software, software tools, training and technical support. Also, the tools should be part of an integrated environment with a universal interface or a collection of standalone tools. Finally, the development environment should include sufficient tools for debugging.

Industrial nets

FROM PAGE 64

of the request, the current time and the length of time for which the ticket will remain valid.

The server adds the random key and the identifying information to the outside of the encrypted packet, encrypts it again with the key of the principal who asked for it and sends it back. The client then decrypts the ticket and sends that to the server. On receiving the ticket, the server decrypts it using the key for its own principal. Given a successful decryption, it can examine the time stamp to see if the ticket is still valid and make a decision about the identity given.

The code and processing overhead is small; Kerberos for an embedded network requires per-

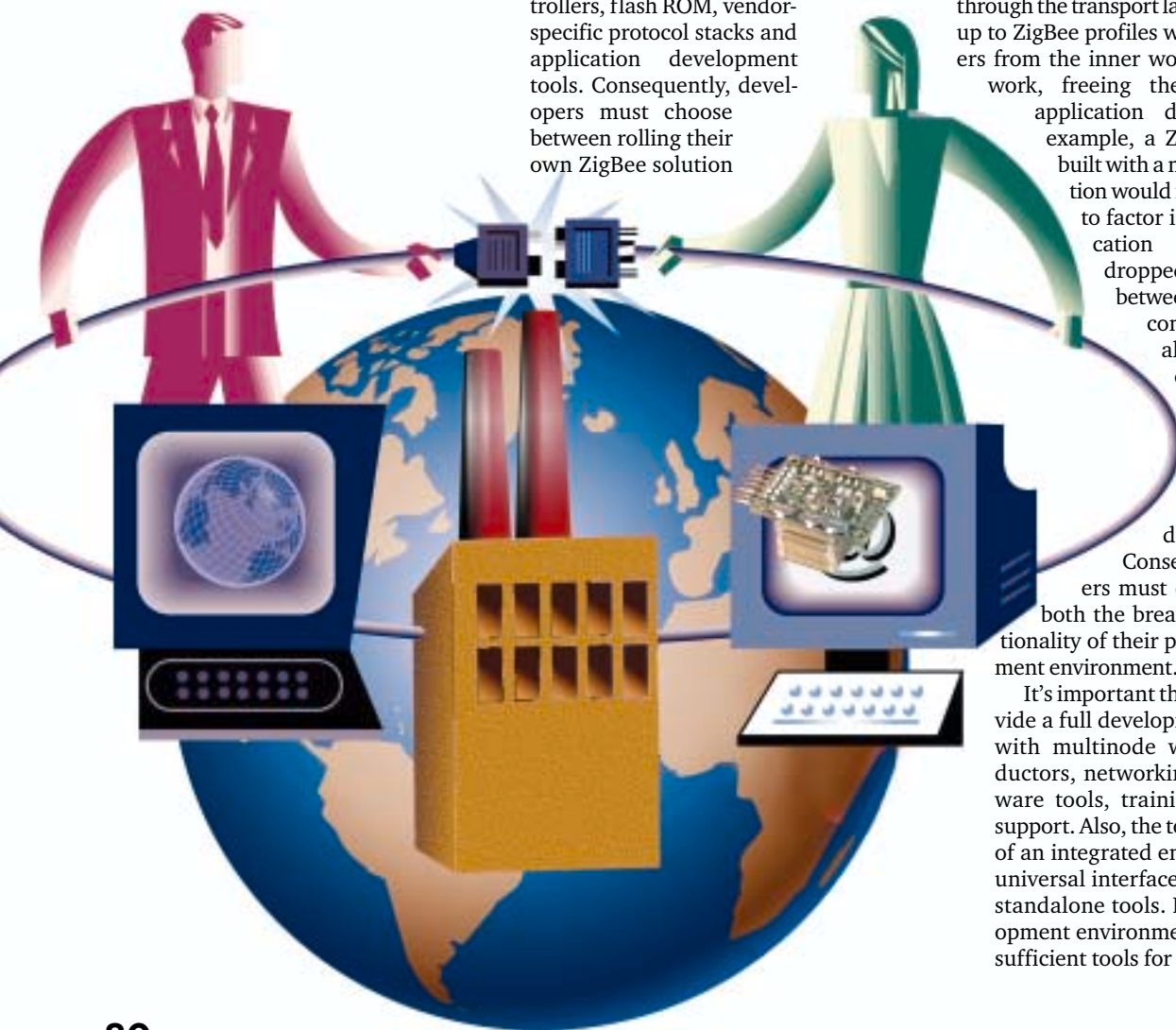
Done right, embedded Ethernet yields unprecedented connectivity.

haps 25 kbytes for code and data, with a relatively small processing overhead on a 32-bit processor. Authentication using a method such as Kerberos helps ensure that unauthorized software or users do not get access to the protocol stream.

Design considerations

Ethernet and standard network protocol stacks such as TCP/IP don't necessarily reduce costs in industrial networks, but their use in such applications will continue to grow. Ethernet solutions require silicon and support materials that combine robust performance and reliability in extreme environmental conditions, accompanied by software solutions that guarantee real-time delivery of data.

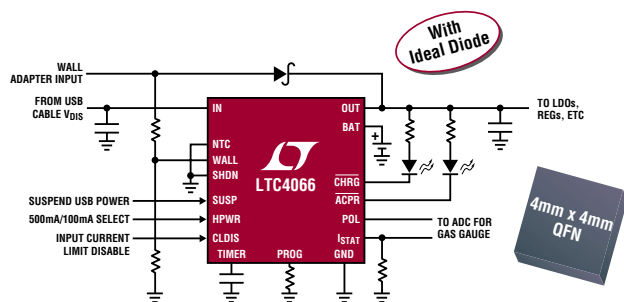
But getting the right combination of cost, standards and features into an embedded Ethernet solution makes it possible to achieve unprecedented connectivity between the factory floor and general-purpose networks. The most common application of this configuration today is remote monitoring, often through Web browsers. The ability to successfully tie together real-time data on manufacturing processes with other business intelligence can offer a powerful boost to productivity and efficiency. Getting device connectivity right is the most important step.



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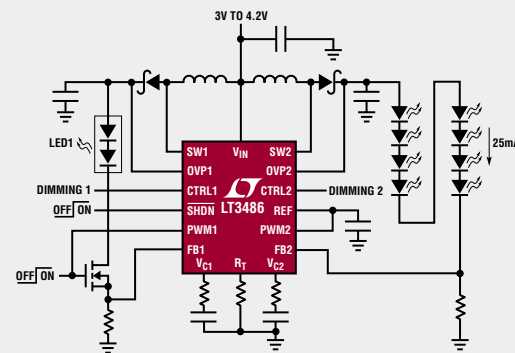
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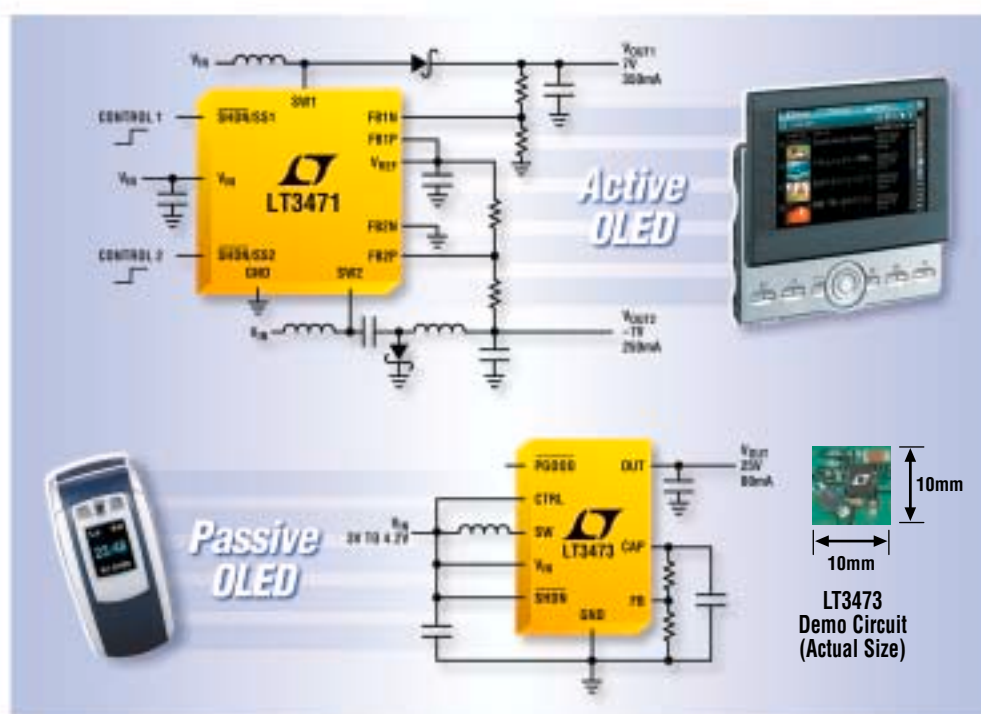
Dual 1.3A White LED Step-Up Converters with Wide Dimming Range—LT3486

Features:

- **Drives Up to 16 White LEDs at 25mA (8 per Driver) from a 5V Supply**
- **Up to 320mA Continuous LED Current per Driver from a Single Li-Ion Cell**
- **Wide (1000:1) Dimming Range**
- **Wide Input Voltage Range: 2.7V to 24V**
- **Available in (5mm x 3mm x 0.75mm) 16-Pin DFN and 16-Pin TSSOP Packages**



OLEDs Driven Here



Efficient and Compact Solutions

Linear Technology offers a broad range of solutions for driving Organic LED displays featuring tiny solution footprints and high efficiency operation. For an Active OLED panel, the LT[®]3471 dual switching regulator with 1.3A switches provides both positive and negative outputs from a tiny 3mm x 3mm DFN package. For Passive OLED panels, the LT3473 is a full featured boost converter with an integrated Schottky diode, 1A switch and true output disconnect during shutdown.

Selected OLED Drivers

Part Number	I _{sw}	V _{IN} Range	Single/Dual	Supply Current	Package
LTC [®] 3459	75mA	1.5V to 5.5V	Single	10μA	ThinSOT™
LT3464	115mA	2.3V to 10V	Single	25μA	ThinSOT
LT3472	250mA/300mA	2.2V to 16V	Dual	2.8mA	3mm x 3mm DFN
LT3473/A	1A	2.2V to 16V	Single	150μA	3mm x 3mm DFN
LT3471	1.3A x 2	2.4V to 16V	Dual	2.5mA	3mm x 3mm DFN

Info & Online Store

www.linear.com

Literature: 1-800-4-LINEAR

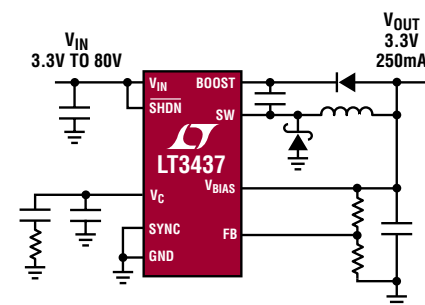
Support: 408-432-1900



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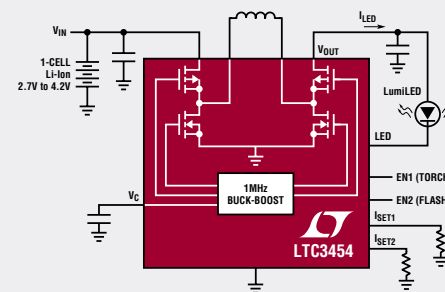
High Voltage 500mA, 200kHz Step-Down Switching Regulator with Only 75μA Quiescent Current—LT3437



Features:

- **Wide Input Range: 3.3V to 80V**
- **500mA Peak Switch Current**
- **Burst Mode® Operation: 75μA Quiescent Current**
- **3mm x 3mm 10-pin DFN Package**

Synchronous Buck-Boost LED Driver Delivers up to 1A to High Current LEDs—LTC3454



Features:

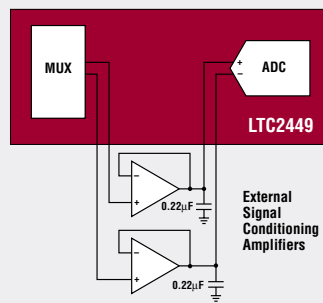
- **High Efficiency: >90% Typical over Entire Li-Ion Battery Range**
- **Wide V_{IN} Range: 2.7V to 5.5V**
- **Up to 1A Continuous Output Current**
- **3mm x 3mm DFN-10 Package**



24-Bit $\Delta\Sigma$ ADC Includes 16 MUX Switches—LTC2444/45/48/49

Features:

- Up to 8 Differential or 16 Single-Ended Input Channels
- Up to 8kHz Output Rate
- Selectable Speed/Resolution $2\mu V_{RMS}$ Noise at 1.76kHz Output Rate $200nV_{RMS}$ Noise at 13.8kHz Output Rate



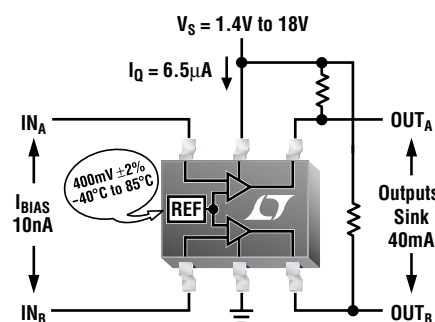
Offsets and 1/f Noise Between MUX and ADC Are Automatically Cancelled

LTC2449: \$7.15 ea. for 1k pc. qty.

Dual Comparator with 400mV Reference—LT6700

Features:

- On-Chip 400mV 2% Reference Over Temp.
- Low Voltage Operation: 1.4V to 18V
- Space-Saving ThinSOT Package
- Open Collector Outputs Sink up to 40mA
- Preset 6.5mV Hysteresis
- Three Input Polarities (-1/-2/-3 Versions)



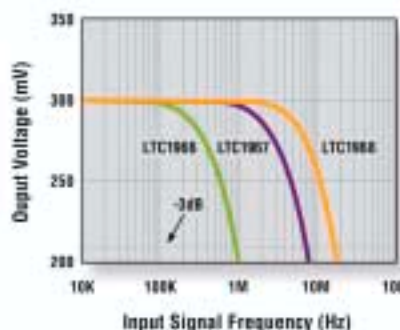
LT6700: \$1.25 ea. for 1k pc. qty.

AC Measurement to 500kHz

Simple

Accurate

Fast



No Drift – Patented $\Delta\Sigma$ True RMS Technology

True RMS is the most accurate technique for measuring an AC signal. And now, it's also the simplest. Linear's newly expanded line of $\Delta\Sigma$ True RMS-DC converters require no in-system calibration for 0.25% low frequency accuracy. This high precision is maintained over the full range of input signal levels, giving these devices unmatched linearity and accuracy – guaranteed over the full industrial temperature range. For AC measurements up to 500kHz, they are simply the best choice.

True RMS to DC Products

Specifications	LTC®1966	LTC1967 NEW	LTC1968 NEW
Bandwidth, 1% Total Error	10kHz	100kHz	500kHz
Typical Linearity	0.02%	0.02%	0.02%
Supply Current	155μA	330μA	2.3mA
Supply Voltage	3V, 5V, ±5V	5V	5V
Input Voltage Range	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
Output Voltage Range	Rail-to-Rail	Rail-to-Rail	Rail-to-Rail
Shutdown	Yes	Yes	Yes
Package	MSOP-8	MSOP-8	MSOP-8
Price (1k)	\$2.95	\$3.40	\$3.95

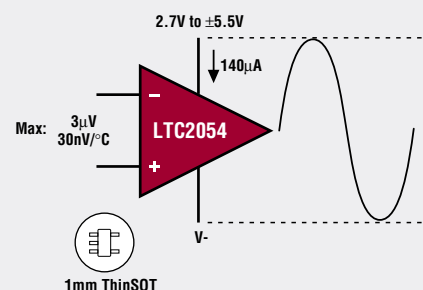
Info & Online Store

www.linear.com
Literature: 1-800-4-LINEAR
Support: 408-432-1900

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Lowest Power Rail-to-Rail Zero-Drift Op Amps—LTC2054

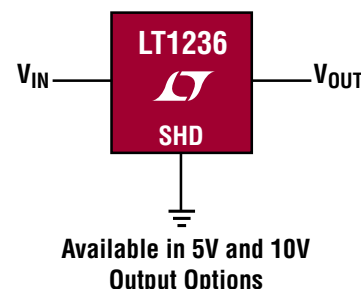


Features:

- $I_S = 140\mu A$
- $V_{OS} < 3\mu V$
- V_{OS} Drift $< 30nV/^\circ C$
- $A_{VOL} = 140dB$
- Rail-to-Rail Output
- ThinSOT™ Package

LTC2054: \$1.00 ea. for 1k pc. qty.

High Precision Reference Operates in Series or Shunt Mode—LT1236



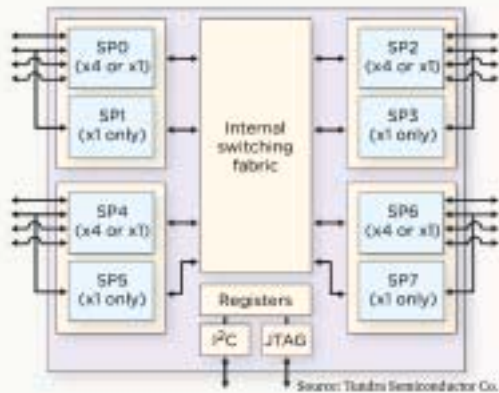
Features:

- Ultra-Low Drift: 5ppm/°C Max.
- Trimmed to High Accuracy: 0.05% Max.
- Excellent Long-Term Stability: 20ppm
- Very Low Noise $< 1ppm_{p-p}$ (0.1Hz to 10Hz)
- Sinks and Sources up to 10mA
- Industrial Temperature Range SO Package

LT1236: \$1.95 ea. for 1k pc. qty.



PRODUCT OF THE WEEK



Tundra's Tsi564A switch packs Serial RapidIO functionality into a smaller (21-mm²) package.

Serial RapidIO switch supports 40-Gb bandwidth

By Ismini Scouras

Ottawa — Tundra Semiconductor Corp. has added a second serial RapidIO switch to its product line—a device it describes as cheaper and smaller than its first offering but able to build the same high-performance communications systems. The Tsi564A, offering low-power multiple port widths and speed configurations and supporting 40-Gbit/second aggregate bandwidth, measures 21 mm². By contrast, the Tsi568A, introduced in February, has a package size of 27 mm².

Based on the Serial RapidIO specification, the new switch incorporates serdes functionality, error recovery, priority-based fabric routing, high payload efficiency and table-based fabric packet routing. In addition, the Tsi564A

CONTINUED ON PAGE 88

Floating-point DSPs tune up audio apps

By Marty Gold

Houston — With a price/performance ratio of up to 130 Megaflops/dollar, Texas Instruments Inc.'s TMS320C6722, TMS320C6726 and TMS320C6727 floating-point digital signal processor chips enable audio engineers to incorporate DSP processing power into a broad spectrum of applications, including broadcast, conferencing, musical instruments and professional audio.

These devices, which are based on TI's latest C67x DSP core, are equipped with the flexible dMAX direct memory access engine, which offloads the processor for specialized off-chip memory accesses during effects processing. The data-movement accelerator DMA engine supports 1-D, 2-D and 3-D transfers and random-off-set multitap off-chip accesses.

The processors also sport new mixed-precision instructions, including 32-bit x 32-bit multiplication with a 64-bit result and 32-bit x 64-bit multiplication with a 64-bit result. This feature improves high-quality FIR and IIR filter performance efficiency in high-sample-rate, low-frequency audio applications, according to TI.

The number of internal registers has doubled from earlier

DSPs, from 32 to 64, to improve performance in register-bound kernels and to make compiler optimizations easier. TI has also doubled the number of concurrent floating-point add instructions from two to four to boost fast Fourier transform processing by 20 percent. Further, the size of the instruction cache has increased from 4 to 32 kbytes, to reduce instruction cache miss penalties.

Together, these additions provide a greater than 20 percent increase in performance for a host of real-world audio applications, TI said. For example, MP3 decoding now requires only 16 MHz on a C672x DSP, down from 20 MHz for the C6713. Also, 10-band equalizer decoding requires 6 MHz on a C672x DSP, down from 17 MHz for the C6713.

The C672x devices range in clock speed from 200 to 300 MHz and come with up to 256 kbytes of SRAM and 32 kbytes of instruction cache. Peripherals were selected specifically with audio applications in mind, the company said. The subset of peripherals varies depending on the specific processor, but the C672x devices include up to three multichannel audio serial ports and a host of other interfaces (two SPI, an HPI,

CONTINUED ON PAGE 88

Switches & relays

By Glna Roos



NKK's E-Series miniature toggles lock out solder flux and other contaminants.

Rugged parts serve in military, industrial apps

Switch and relay manufacturers are beefing up their component offerings with devices that meet demanding requirements in industrial and military applications. Parts designed for these harsh applications often must meet the toughest environmental requirements, such as protecting against water, heat, solvents, dust, dirt and other contaminants. In many cases, they also need to offer long mechanical life and resistance to shock and vibration.

In the past six months, switch and relay makers such as Bergquist, EAO Switch, Electroschalt, Gigavac, ITT Cannon, NKK, Tyco and Waytek have rolled out new offerings that can withstand tough environments.

For industrial applications, Tyco Electronics Corp. offers its Kilovac EV200 series. Developed for explosive and harsh environments, the hermetic

CONTINUED ON PAGE 84

REVIEW OF THE WEEK

Adlink card shows GPIB interface for test apps

PCI-compatible unit works in most desktop computers

Irvine, Calif. — Adlink Technology Inc. released its first PCI IEEE 488 controller card. The PCI-3488 links General Purpose Interface Bus instruments and PCI-equipped systems via an interface that is compliant with IEEE488.1 and IEEE488.2 standards. The card is being offered at an introductory price of \$240 until Aug. 31.

The PCI-3488 is 32-bit/33-MHz PCI-compatible and represents Adlink's innovations in PCI adapter hardware design. The PCI interface supports both 3.3- and 5-volt PCI environments to make it suitable for most desktop computers and



Controller card supports such application development environments as Delphi and LabView.

REVIEW CONTINUED ON PAGE 90

eeProductCenter's Alex Mendelsohn files his review

Although the Universal Serial Bus is increasingly being used to glue test systems together, the tried-and-true IEEE-488 General Purpose Interface Bus is still widely deployed, and there are lots of legacy GPIB-compatible instruments out there. Thus, Adlink Technology's PCI-3488 IEEE-488 controller card is a viable product with potentially wide appeal. Once installed in a host PC, it can control up to 14 IEEE-488.2-compatible instruments, with high throughput.

With a National Instruments-like driver application programming interface

➤ eeProductCenter is happy to present its May Product of the Month award to Altera Corp. (San Jose, Calif.), for Altera's FPGA-based video-over-Internet Protocol reference design. The selection was based on the largest number of page view clicks to our Web site over the past month. For more information on the product, search www.eeProductCenter.com for article ID: 160700355.

Components

Mil-duty devices

FROM PAGE 83

cally sealed relays are said to be intrinsically safe, with no oxidation or contamination of coils or contacts. They also provide stable contact resistance over years of use, including long periods of nonoperation, the company said. The relays offer high contact ratings for their size and target several industrial applications, including battery switching and backup, dc voltage power control, circuit protection and safety applications. Mechanical life is rated at 1 million cycles. (For more details, search www.eeProductCenter.com for article ID: 161601557.)

Also eyeing industrial applications, Electroswitch Corp. offers a large selection of heavy-duty devices that include detent-, snap- and cam-action rotary switches as well as tap and knife switches. The company said that all of its industrial switches come with long-life contacts for trouble-free service and reliable performance under severe shock and vibration. Many models are available in keylock, gear-driven and application-specific cus-

tom configurations. (Search www.eeProductCenter.com for article ID: 60407868.)

EAO Switch Corp. also offers a wide range of stainless-steel switches, keypads and keyboards for industrial applications in harsh environments. These devices offer IP67 protection against water, heat, shock, vibration and vandalism, and they require minimal maintenance, according to the company. Several devices have protective front rings and bezels, which suit them for operation in wet or dusty environments and offer additional protection against vandalism, harsh usage and aggressive cleaning. (Search www.eeProductCenter.com for article ID: 59200247.)

For security applications that must withstand vandalism and harsh usage in difficult environmental conditions, EAO Switch has developed several new switch lines that fit the bill. Most recently, the company has expanded its suite of security options for its broad range of keylock switches. The new models offer optional security features that protect against unauthorized access and offer higher levels of safety control.

Capable of withstanding harsh environments, the keylock switches are built from high-quality materials and are tested to meet many international standards, including IP67, the company said. They can also be supplied with a flush mount to protect



EAO's keylock switches, with an expanded suite of security options, meet international standards such as IP67.

against vandalism. (Search www.eeProductCenter.com for article ID: 60404160.)

EAO's Series 61 switches, meanwhile, meet IP65 front-protection standards. The 16-mm oil- and watertight switches are available in a choice of actuators, including pushbuttons, indicators, keylocks and selector switches as well as EN-418-rated emergency stops. The switches can be used to retrofit existing control panels or for new designs, particularly in machinery, process control, medical equipment and instrumentation. (Search www.eeProductCenter.com for article ID: 49901859.)

Light-duty toggles

Switches featuring several protective features are available from NKK Switches Inc. For example, the E-Series of light-duty miniature toggle switches includes a high-torque bushing that prevents rotation and separation from the metal frame during installation, as well as a stainless-steel frame to resist corrosion. An anti-jamming design protects the contact mechanism from damage if the lever is subjected to a sharp downward force or other harsh treatment, NKK said. In double-pole models, higher-insulating barriers protect the toggles against crossover. Solder lug or straight pc terminals are standard and are epoxy-sealed to lock out solder flux and other contaminants. (Search www.eeProductCenter.com for article ID: 60404161.)

Similarly, NKK's M2B series of process-sealed miniature pushbutton switches includes several design features to lock out contaminants. These include an interior O-ring surrounding the actuator within the bushing, ultrasonic welding of the bushing and housing unit, and epoxy-sealed terminals. The single-unit construction of the bushing and top of the housing provides added protection from cleaning fluids or other liquids. (Search www.eeProductCenter.com for article ID: 54200586.)

Touting weather resistance, Berg-

quist Co.'s latest membrane switches can be used in harsh environments and are said to operate underwater, in the rain or snow, and at high and low temperatures. They also continue to function after exposure to harsh chemicals and solvents, the company said. Bergquist's HeatSeal process allows the switches to be designed into almost any environment, according to the company. (Search www.eeProductCenter.com for article ID: 56900275.)

A series of switches from Waytek Inc. is also billed as completely weatherproof and sealed from the environment. The toggle switches feature a weather-resistant plastic coating with an O-ring seal. (Search www.eeProductCenter.com for article ID: 49900549.)

For military use, Electroswitch has launched its Series 24G, comprising instrument and control switches that withstand harsh military applications. The products are available with a choice of electrical ratings that include 20 amps, 500 volts (continuous); 20 A, 125 Vac resistive (inductive); 10 A, 250 Vac resistive; 5 A, 500 Vac resistive, and 0.4 A, 350 Vdc resistive.

The rotors (movable contacts) are made of silver-overlay phosphor bronze; the stators (stationary contacts) are silver-overlay copper, and spacers are glass-filled alkyd. Waterproof mounts are available. (Search www.eeProductCenter.com for article ID: 51202833.)

Another tough switch series comes from ITT Industries Electronics Components. The AR4 and AR5 analog rocker switches feature a contactless sensing design that provides an accurate, proportional output suitable for off-road machinery, the company said. The devices tout a life of more than 1 million cycles (some 1.5 million cycles for the AR4) and deliver the reliability required for applications in demanding environmental conditions.

Both the AR4 and AR5 switches meet rigorous electromagnetic-compatibility and mechanical-vibration standards. They have also been tested to withstand salt spray and chemical-splash tests (SAE J1455 4.3.3). The AR4 series is protected to IP67, and the AR5 meets IP65 requirements. (Search www.eeProductCenter.com for article ID: 159901780.)

For tough relays, Gigavac says its G71 single-pole, 70-kV relay is safe in nearly any environment and can perform where others fail. Filled with SF6 gas for low leakage and high-current capacitive-discharge switching, the relay is not affected by humidity or dust, and it can operate from -50°C to 85°C, according to Gigavac. (Search www.eeProductCenter.com for article ID: 57701225.)

Clearly, switch and relay makers will continue delivering the reliability required for the most demanding requirements with unique features that protect against severe environments and harsh usage.



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Components

Mini relay recognized by Underwriters' Laboratories

Maple Grove, Minn. — CIT Relay & Switch has introduced the WJ105E/J105E series of lightweight, miniature RoHS-compliant relays with UL/cUL recognition. These devices may be used in air conditioners, refrigerators, microwave ovens, heaters and HVAC controls, the company said.

Designed for compact mounting, the relays offer numerous choices in coil voltages from 3 to 48 Vdc. Available in normally open, single-pole/single-throw or single-pole/double-throw contact arrangements, the relays are offered in ratings of 10 amps at 125 Vac, 1/4 hp at 120/250/277 Vac, 4.2 A at 277 Vac, 5A at 250 Vac, TV-5 at 120 Vac and Pilot Duty (C150). Coil power choices include .2 and .45 watt, providing low coil power consumption with the 10-A switching capability.

The relays provide 8,000-V surge voltage between contacts, insulation resistance of 100 mW minimum at 500 Vdc and dielectric strength (at sea level) of 4,000 Vrms minimum, coil to contact, and 1,000 Vrms minimum, contact to contact.

The relays are sealed and can withstand soldering and wash cycles including wave solder at up to 265°C and reflow solder up to 260°C. Electrical life is rated at 100,000 cycles and mechanical life at 10 million cycles. Pricing starts at 69 cents in quantities of 1,000, depending on contact and coil arrangement. Delivery is from stock to 10 weeks. The optional RoHS-compliant part is available as the J105E series.

Call (763) 535-2339

Search www.eeProductCenter.com for article ID: 163105303

Connectors enable port selection in HDD carriers

Etters, Pa. — FCI has developed a line of 29-position serial-attached SCSI (SAS) plug and receptacle connectors and 22-position serial ATA (SATA) receptacle connectors for port selector assemblies in removable hard-disk-drive (HDD) carriers used in enterprise servers and storage systems. Options for vertical or right-angle connector terminations are available, which lets engineers tailor the orientation of the internal pc board to the drive's form factor.

Vertical connectors position the port selector pc board assembly perpendicularly to the device plug on the HDD, which may be preferred with a 3.5-inch drive. Using right-angle connectors allows the pc-board assembly to be positioned parallel to the device plug on the HDD. This orientation may be useful when developers need a larger pc board for the smaller 2.5-inch drive. The SAS plug and receptacle connectors work with the European Union's Restriction of Hazardous Substances directive.

"The SAS plug connector on the port selector pcb assembly provides two ports at the interface between the drive carrier module and a SAS backplane receptacle," said David Sideck, FCI regional market manager, in a statement. "At the HDD interface within



FCI is targeting removable hard disk drive carriers for its new connector offerings.

the drive carrier, there are two options. Use of a SAS receptacle provides two ports and the capability to accept either SAS or SATA drives. A SATA receptacle supplies a single port and accepts a SATA drive, but the connector is keyed to block the installation of a SAS drive."

Typical prices range from \$1 to \$1.50 each in lots of 1,000, depending on the connector type and configuration. Samples are available. Delivery for production quantities is stock to four weeks.

Call (800) 237-2374

Search www.eeProductCenter.com for article ID: 163105999

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Certification

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Wirewounds dissipate less

Boone, N.C. — Providing designers with cost-effective resistors for power circuits where board space is tight, resistor maker IRC offers wirewound devices that are rated at double the power dissipation of traditional axial-leaded packages. Designated the SP and SPP series, these power wirewound resistors are also available in fusible and flame-resistant versions.

Applications for the SP and SPP series resistors include power supplies, motor controllers, TVs and consumer electronic products and appliances as well as general-purpose power circuits. The resistors can also be used as drop-in replacements for carbon-composition devices in certain cases.

The SP20 series is rated for 1 W at 50°C, with resistance values from 0.1 ohm to 1,200 Ω, in standard tolerances of ±5 percent and ±10 percent, with temperature coefficient of resistance (TCR) ratings as low as ±150 ppm/°C. The SPH series is rated for 2 W at 70°C, with resistance values from 0.1 Ω to 2,400 Ω, in standard tolerances of ±5 percent and ±10 percent, with TCRs as low as ±150 ppm/°C.

The SP20 series is rated for 1 W in

a package typically associated with half-watt devices, while the SPH line is rated for 2 W in a 1-W package. The SP20, SP20F, SPH and SPF devices are built with a metal alloy resistance wirewound wrapped around a fiberglass core. They have welded end caps and are sealed with a molded phenolic material. They are also marked with solvent-resistant color bands.

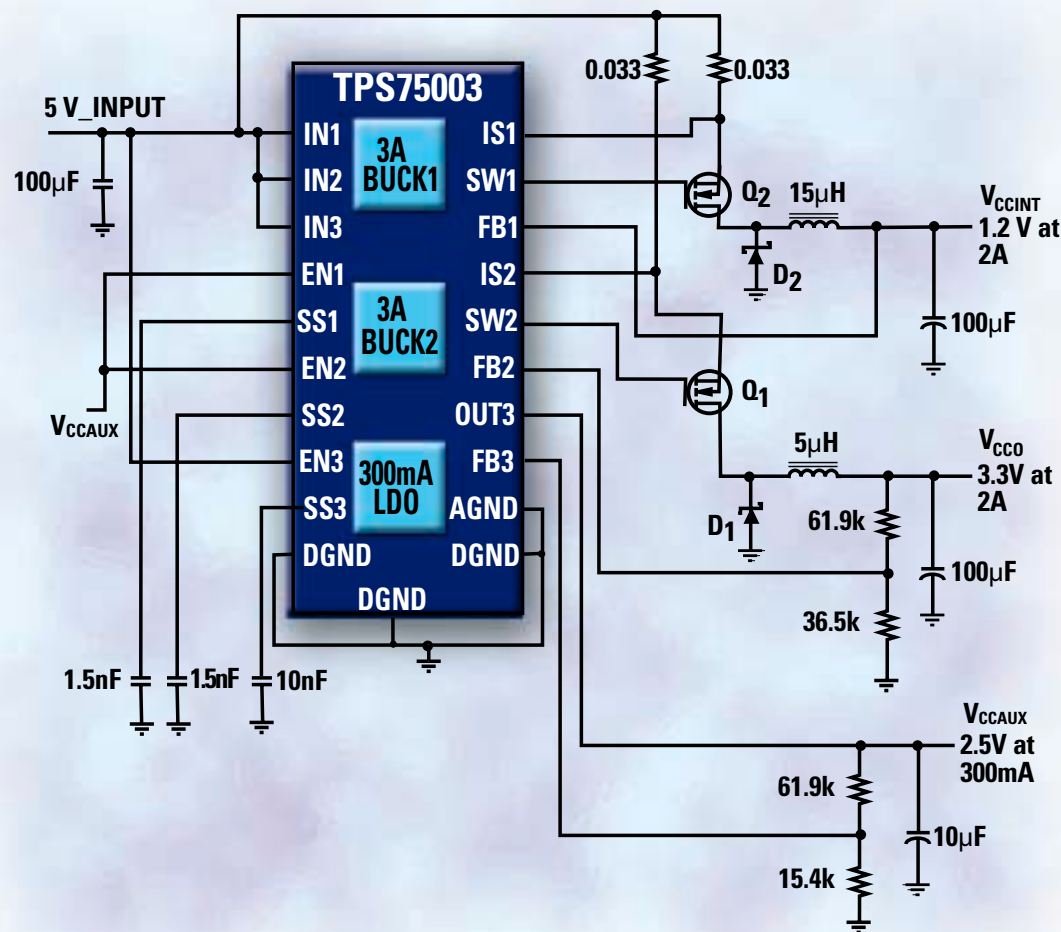
The SPP series resistors are rated for 1 W, 2 W and 3 W at 85°C, with resistance values from 0.1 Ω to 2,400 Ω (lower ranges available), in standard tolerances of ±5 percent and ±10 percent, with TCRs as low as ±300 ppm/°C. They are built with a metal alloy resistance wirewound around a fiberglass core with crimped end caps, conformally coated and marked with solvent-resistant color bands.

Typical pricing for the SP20 and SPH series resistors is 13 cents to 19 cents each in quantities of 10,000. The SPP series resistors are typically priced at 10 cents each in lots of 10,000. Delivery is stock to six weeks.

Call (828) 264-8861

Search www.eeProductCenter.com for article ID: 163106006

Triple Supply Powers Spartan™-3



► Applications

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- Set-top boxes
- Plasma TV display panels
- DVD players

► Features

- Two 95%-efficient, 3-A buck controllers and one 300-mA LDO
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 - from 1.0 V for LDO
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- Independent soft-start for all three power supplies
- LDO stable with small ceramic output capacitor
- Independent enable for each supply for flexible sequencing
- 4.5 mm x 3.5 mm x 0.9 mm 20-pin, QFN package
- \$1.90: 1 K price

The **TPS75003** power management IC for Xilinx's Spartan™-II/IIE/3 series of FPGAs integrates multiple functions to significantly reduce the number of external components required and simplify design. Combining increased design flexibility with cost-effective voltage conversion, the IC includes programmable soft-start for in-rush current control and independent enables for sequencing the three channels. The TPS75003 meets all Xilinx startup profile requirements, including monotonic ramp and minimum ramp times.

For more information on TI's complete line of power management solutions for Xilinx FPGAs—including a library of reference designs, schematics and BOMs—visit www.ti.com/xilinuxfpga-u.



www.ti.com/xilinuxfpga-u • 800.477.8924, ext. fpga

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TEXAS INSTRUMENTS

Chips

Log amp senses 1 MHz-10 GHz

Norwood, Mass. — Analog Devices Inc. has released an RF logarithmic detector/controller that claims to accurately measure the power of radio signals from 1 MHz to 10 GHz, covering all cellular standards and a variety of wireless infrastructure and broadband wireless appli-

cations. The device comes in a 2 x 3-mm package and consumes only 20 milliamps (less than 1 mW when disabled), suiting it for portable applications.

The AD8317 offers accurate RF measurement of better than ± 1 dB over a dynamic range of more than 50 dB and can function as a power controller when its outputs are used to adjust a power amplifier or a variable-gain amplifier. The 1-MHz to 10-GHz operating frequency range supports all cellular standards (GSM, CDMA, wide-band CDMA and TD-SCDMA), broadband wireless standards (802.16, WiMAX, WiBro) and proprietary systems that operate in a variety of frequency bands.

The log amp provides precise, temperature-stable performance over the full range of -40°C to 85°C . Its output response time of 5 nanoseconds enables RF burst detection to beyond 125 MHz. It operates over a supply voltage range of +3 to +5 Vdc. The AD8317 is priced at \$3.93 per unit in lots of 1,000 and is packaged in an eight-lead LFCSP. It is sampling now, with volume production set for October.

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Rotary encoder IC suits motion-sensing apps

Unterpremstaetten, Austria — Austriamicrosystems' magnetic rotary encoder IC for industrial and automotive motion-sensing applications provides an analog voltage proportional to the measured angle, in addition to 10-bit digital position information. Users can program the device to operate within a predefined, application-specific angle range. Depending on the angular range settings, the step size of the analog output may vary from 0.35° to 0.09° per step.

The IC outperforms current motion-sensing solutions, such as high-end potentiometers, in reliability and lifetime because of its contactless sensing method, said Ralf Kodritsch, marketing manager for sensors and automation at Austriamicrosystems.

The device also offers zero-position programming and diagnostic features. It provides a warning in the event of a power loss.

The user can select for optimized operation at either high speed or high accuracy. The daisychain mode allows

the connection of several devices in series over a two-wire bus.

The magnetic rotary coder IC operates at either 3.3 or 5 volts and over a temperature range of -40°C to 125°C . The AS5043 is available in a lead-free



Users can program the AS5043 to suit the angle range to the application.

SSOP-16 (5.3 x 6.2 mm).

Product samples will be available in June. Pricing is \$4.50 in 1,000-unit quantities.

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for article ID: 163700277

Serial RapidIO

FROM PAGE 83

supports RapidFabric extensions, including data-streaming packet switching for encapsulation.

RapidIO is a packet-switched, interconnect and fabric technology that addresses the embedded industry's need for increased bandwidth and faster buses. Designed to enhance the performance of communications processors, host processors and networking digital signal processors, it allows chip-to-chip and board-to-board communications at performance levels scaling to 10 Gbits/s and beyond.

The Tsi564A goes beyond standard specification requirements to solve system-

level issues with low power consumption and hot-swappable I/Os, Tundra said. The extensive buffering and traffic management architecture is designed for line-rate termination and the prevention of head-of-line blocking.

PCI Express, the next-generation serial-bus interconnect standard, is challenging widespread adoption of RapidIO. PCI Express is the dominant bus standard in computing applications, while RapidIO is designed for networking, storage and communications systems. However, as microprocessor clock speeds continue to increase, RapidIO proponents say that bus architectures cannot meet system bandwidth requirements.

Texas Instruments Inc. is also supporting RapidIO and recently introduced the

TMS320C6455—the first DSP developed using serial RapidIO technology.

Paul Mesibov, director of engineering at Pentek Inc., a maker of advanced analog and digital I/O products, said that Tundra's Tsi564A serial RapidIO switch "provides the performance required by increasing I/O bandwidth found on next-generation processors. The Tsi564A switch and TI's C6455 DSP provide a range of solutions that optimize performance, power efficiency and the flexibility required for our next-generation platforms."

The Tsi564A will be available in June for less than \$59 each in volume, compared with \$99 for the Tsi568A.

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DSPs for audio

FROM PAGE 83

an RTI, an EMIF and two I²C), as well as a phase-locked loop. The DSP's core is a C-efficient VLIW architecture.

TI is simultaneously launching a Professional Audio Development Kit (PADK) from Lyrtech Signal Processing. The PADK lets developers quickly evaluate C672x device performance and begin product development immediately, without having to first craft their own prototype board, TI said. The PADK integrates the C6727 DSP with



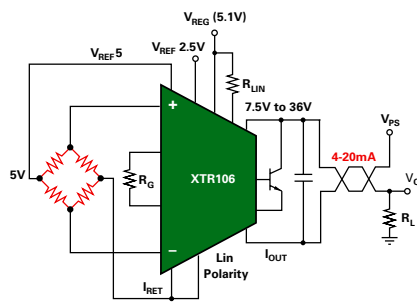
TI development kit from Lyrtech helps users evaluate C672x device performance.

TI's complementary analog technology, including A/D and D/A converters from the company's Burr-Brown product line, and it is tuned for high-end

pro-audio applications. An on-board expansion slot provides flexible I/O connectivity and enables developers to evaluate other analog components.

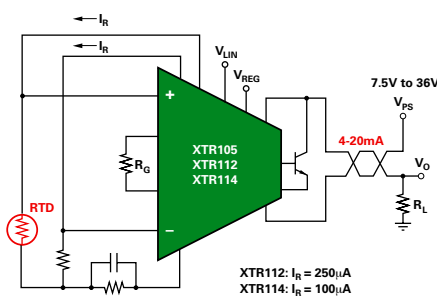
The devices are sampling now, with production slated for the fourth quarter. The C6722 DSP at 200 MHz is priced at \$9.95, the C6726 DSP at 250 MHz is priced at \$14.10 and the C6727 DSP at 300 MHz sells for \$19.95, all in production volumes. The PADK is also available now from Lyrtech at \$1,995. TI will begin selling the kit in the third quarter.

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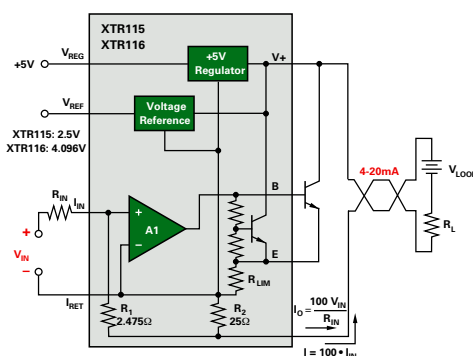
► 4-20mA Current Transmitter with Bridge Excitation Linearization (XTR106)

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- Auxiliary output: 5.1V at 1mA
- Bridge linearization circuitry
- Packaging: DIP-14, SOIC-14
- Price: \$4.00 in 1k qty



► 4-20mA Transmitter with RTD Conditioner (XTR112, XTR114, XTR105)

- Loop voltage: 7.5V to 36V
- Full scale input: 5mV to 1V
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 - XTR105: 800μA (100Ω RTD)
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 - XTR114: 100μA (10kΩ RTD)
- RTD linearization circuitry
- Packaging: DIP-14, SOIC-14
- Price: \$4.00 in 1k qty

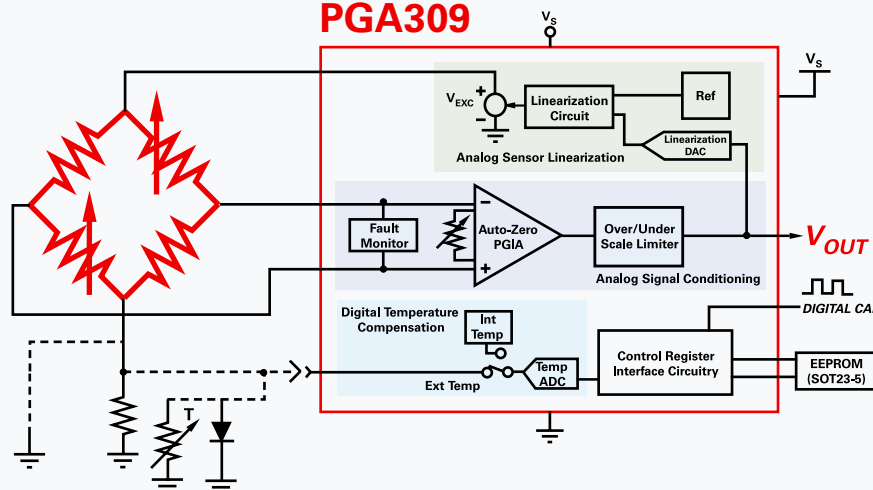


► 4-20mA Transmitter with 200μA Low Quiescent Current (XTR115)

- Loop voltage: 7.5V to 36V
- $I_O = I_{IN} \times 100$
- Subregulated output: 5V at 4mA
- Reference output:
 - XTR115: 2.5V at 2.5mA
 - XTR116: 4.096V at 2.5mA
- Packaging: SOIC-8
- \$1.05 in 1k qty

Complete Bridge Sensor Conditioner

PGA309



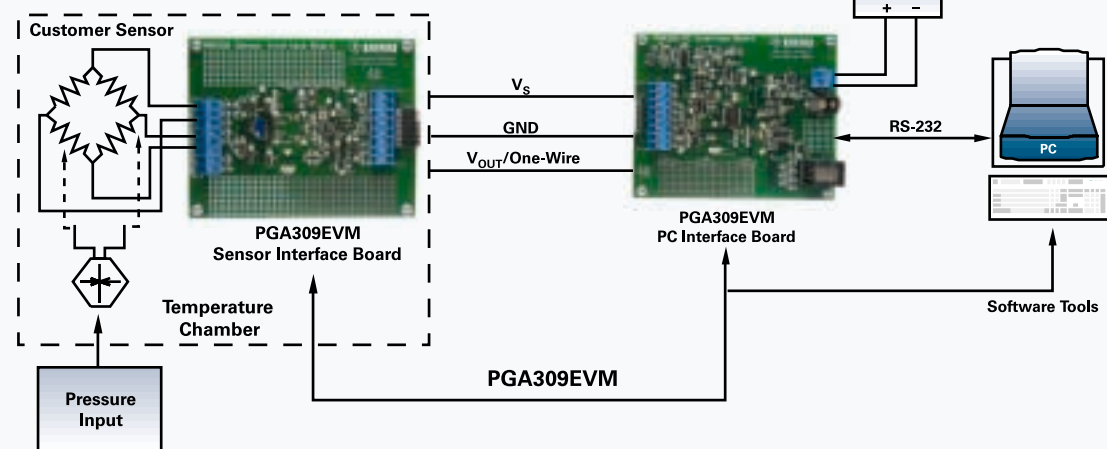
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Software Tools

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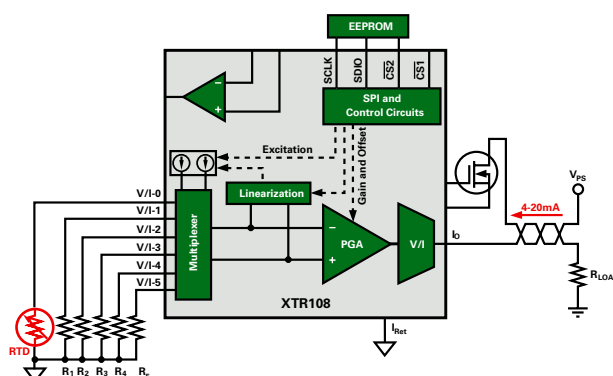
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- Digital calibration/configuration
- Subregulated output: 5V
- Reference output: 1.2V
- Packaging: SSOP-24
- Price: \$3.35 in 1k qty
- Designers kit available: XTR108DK



Subsystems

Mezzanine card imparts high-res 2-D/3-D graphics

By Alex Mendelsohn

Nuremberg, Germany — A PMC graphics mezzanine card from board maker MEN Micro Inc. gives users a way to include high-resolution 2-D and 3-D graphics in systems that accommodate PMC cards. Typical systems include those based on VMEbus, CompactPCI and PXI. The board will also work in bus-independent systems.

At the heart of MEN's P517 PMC card is an SM731 graphics controller chip from IC maker Silicon Motion Inc. The device is capable of a maximum resolution of 1,600 x 1,200 pixels, with as many as 16.7 million colors. It gives the board a maximum refresh rate of 85 MHz.

The P517 can control thin-film-transistor LCDs, CRTs or standard television screens. Two low-voltage differential-signaling (LVDS) channels, with a maximum pixel clock speed of 112 MHz, can be used either to drive two distinct

screens or a single high-resolution UXGA panel. The P517's two LVDS channels are accessible through an on-board connector or a rear-panel connector found on the P517's carrier board.

Multiple connectivity options on the P517 also allow developers to integrate high-resolution graphics into industrial systems. For example, a DVI-I (digital video interface) for analog and digital LCD and CRT screens, as well as PanelLink, is available on the P517's front panel. In addition, S-Video inputs and outputs, and a composite video output, are also located on the front panel.

Pricing for the graphics mezzanine card starts at \$594 for single units. In the United States, MEN Micro products are sold through a national network of technical manufacturers' representatives. Call (512) 267-8883

Search www.eeProductCenter.com for article ID: 59300572

REVIEW OF THE WEEK

FROM PAGE 83

Adlink's release

industrial PCs. A 1-kbyte on-board FIFO and high-speed bus, accelerated by an on-board complex programmable logic device, give the card a 1.5-Mbyte/second maximum data transfer rate to satisfy high-volume data transfer requirements.

The controller card has been hardware- and software-verified with a wide range of products and applications. It supports popular application development environments such as VB, VC, Delphi and LabView and features a "drop in" system configuration for compatibility with existing test-and-measurement applications.

The PCI-3488 supports Windows 98, NT, 2000 and XP, and its driver library is compatible with industry-standard Virtual Instrument Software Architecture and instrumentation protocols.

The PCI-3488 ships from stock, with OEM volume discounts available. Call (866) 4-ADLINK www.adlinktech.com

Alex Mendelsohn's review

and Virtual Instrument Software Architecture (VISA) support, the fast PCI-3488 also ensures compatibility with existing applications and instrument drivers. Its driver API is binary-compatible with NI's GPIB library through GPIB-32.DLL, so all programs written based on the GPIB-32.DLL can be executed on the PCI-3488 without modification.

Similarly, the VISA library support can be used with most common instrument drivers written by instrument vendors. Not mentioned in the company's press release is that the board will also work with the Agilent IO Library.

The PCI-3488 card ships with an interactive Windows utility program that aids in quick card test and diagnostics. Put all of that together, factor in the special offer of \$240, and it's a compelling package.

For the full text of this review, please search www.eeProductCenter.com for article ID: 163105830.

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Power Products

Astec's three-phase supplies raise DIN to 960 W at 24 V

Carlsbad, Calif. — Astec Power's three-phase model additions to its ADN Series of rugged (ac/dc) switching power supplies extend the family's power capability—up to 960 watts at 24 volts.

The new models, rated from 120 W, mount conveniently on standardized DIN rails in industrial enclosures. Suited for factory automation and other industrial applications, the ADN Series models can accommodate the large peak loads needed to run motor controllers and other devices with high surge-current demands. The supplies are rated for operation to +60°C with no derating.

The models feature nominal output current ranges from 5 to 40 amps, and all of the supplies can support up to double their rated current for up to two seconds. The supplies sport a user-friendly front panel with adjustable voltage control, parallel operation switch, convenient input/output connections and dc

status indicator along with easy-mounting hardware on the rear for DIN-rail installation.

The supplies feature an efficiency of greater than 90 percent. The units are approved for use in Class 1, Div 2 hazardous locations and meet the SEMI F47 standard requirements for voltage sag immunity in semiconductor fabrication equipment. All models incorporate power factor correction and autoselect of input voltage between 340 and 576 Vac.

The product's data sheet is available at www.astecpower.com/products/data_sheets/DC-DC/ADN_3-phase.pdf. Backed by a three-year warranty, the products meet international safety and performance standards including listings from UL and CE. Samples are available now with prices starting at \$150 each for the 120-W model.

Call (760) 930-4600

Search www.eeProductCenter.com for article ID: 162100833

Programmable loads can heft nearly 2 kW

Elgar's series of electronic loads comes in modular and rack-mount versions

San Diego — Power supply vendor Elgar Electronics Corp. is rolling out its first commercially available electronic loads. Offered in both modular and rack-mount configurations, the SL Series units provide a selection of loads for dc and ac inputs, with versions capable of handling between 75 watts and 1.8 kW.

Thanks to their modular architecture, the SL Series loads are also upgradable and expandable to adapt to changing requirements, according to the company.

In use, a control system lets the designer control the loads in one of three ways: through the front panel; via IEEE-488/GPIB or RS-232 serial I/O; or with an analog input. That control flexibility makes the SL Series suitable for applications in automatic test equipment, process control and re-

search, according to Elgar.

The loads are offered in 60- to 500-volt models with a four-bay chassis. Any combination of modules can be configured in a mainframe chassis.

The SL Series is available in three families: SLM, SLD and SLH.

The SLM is a single-input family with ac and dc models. The SLD has dual dc inputs. All modules are modular loads that fit into a single-bay or four-bay mainframe.

For its part, the SLH family offers higher power ratings, from 600 to 1,800 W, as single-input loads, with five ac and six dc models. SLH models are in a common 4U-size, 19-inch rack-mount frame.

All SL models come with a CE Mark declaration and a one-year warranty. Pricing for configured chassis with four modules starts at about \$4,900. Benchtop unit pricing starts at \$1,350 and rack-mount units start at about \$2,900. Call (800) 733-5427

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JUNE
8

Analog eLab: Utilizing High-Speed ADCs for Undersampling

— 9:00 am PT/12:00 pm ET

Texas Instruments and Memec/Insight Electronics

Using high-speed A/D converters to digitize input frequencies above a converter's baseband region (dc to $f_s/2$) is gaining much popularity in communications applications. In many applications the intermediate frequency (IF) can be as high as 250MHz — a frequency usually too high to digitize in an oversampling process. Join TI's Bill Klein for an engaging discussion on undersampling, or as it is sometimes called, direct-IF down conversion. Learn how undersampling can help you to reduce component count and eliminate a complete analog down conversion stage. ■

JUNE
8

Discover Microsoft Windows Embedded – Technical Overview of Hardware Support, Shared Source, Power Management, Server Support, and More.

11:00 am PT/2:00 pm ET — Microsoft Corp.

Find out why Windows Embedded operating systems are right for your next embedded project. Windows Embedded operating systems are used in a range of devices-from PDAs to Industrial Controllers. We'll discuss the operating systems and expert tools that power the Windows Embedded Family specifically Windows CE, the hard real-time operating system built from the ground up for small-footprint devices, and Windows XP Embedded the componentized version of Windows XP Professional. ■

JUNE
15

PLD Design In a Pb-Free World

11:00 a.m. PT/2:00 p.m. ET — Lattice Semiconductor

The compliance deadline for the European Community Directive on RoHS (Reduction of Hazardous Substances) is looming just 14 short months from now with lead-free PCB design a critical element of the change. What does it take to upgrade existing designs to RoHS-compliant? What issues and specifications should you as a designer be concerned about during this upgrade process? ■

JUNE
16

Optimizing Power Consumption In Embedded Systems Using ARM®-Based Microcontrollers From STMicroelectronics

9:00 am PT/Noon ET — STMicroelectronics

Designed for a wide range of applications, STMicroelectronics' family of ARM-based microcontrollers, STR7 with 9 available versions, offers several versatile low-power modes, best-in-class Flash memory performance for fast deterministic applications, best-in-class Flash-to-RAM ratio, Read-While-Write Dual Bank Flash, a powerful set of peripherals including USB, CAN, multiple UARTs, I2C, SPI, and HDLC, as well as an embedded 1.8V core regulator. ■

JUNE
22

Virtuoso Wireless Design Flows—RF IC and System/IC Designs

11:00 am PT /2:00 pm ET — Cadence Design Systems

Today's custom design teams are facing greater market demands, tighter schedule, and ever increasing design complexity and physical effects. Sign up for the Virtuoso wireless design flow webinar and learn about the key elements of an effective wireless design flow and address specific challenges with a methodology that reduces risk in your design techniques. ■

JUNE
22

Learn How Easy It Is To Build an OS Image With Microsoft Windows Embedded

11:00 am PT/2:00 pm ET — Microsoft Corp.

See how easy it is to build a WE image for your next embedded project. See the steps for analyzing the underlying hardware, configuring, building, downloading and debugging a Windows CE 5.0 and a Windows XP Embedded with Service Pack 2 operating system image. Learn to pre-configure platforms for a broad range of devices and see how using Windows Embedded Studio tools allow you to easily customize any of the over 12,000 components that make up Windows XP Embedded. ■

Electronics Supply & Manufacturing Editorial NetSeminar

JUNE
8

Applying Lean Principles To The New Product Development Process

2:00 pm ET/11:00 am PT — Oracle

You've heard of Lean Manufacturing and Lean Supply Chain Management. Well now get ready for the application of Lean principles to Design and New Product Development. As many electronics companies trim R&D budgets, outsource design and purchase IP like a commodity, the design and product development process is becoming more complex. Lean principles can help improve the end-to-end new product development process.

Join Bruce Rayner, editor-in-chief of *Electronics Supply & Manufacturing*, and guests from the industry as they discuss the application of Lean principles to design and product development, including results from a new reader survey. ■

TTI Technical Seminar Series

JUNE
9

Connectors: The Need For Speed

9:00 am PT/Noon ET — TTI, Inc.

So many options, so little time. What will work best for you? Tune in as the industry's authority on connectors, Bob Hult of Bishop and Associates, Inc., along with experts from FCI, Molex and Tyco offer some invaluable advice on high speed backplane connectors. ■

Be Smart -
Choose the
Right Parts

JUNE
23

Analog Devices Presents...INTEGRITY RTOS and Blackfin Processors for Security, Reliability or Time To Market. Who Says You Have To Choose?

12:00 pm ET/9:00 am PT — Analog Devices Inc, Arrow Electronics and Green Hills Software

Are your embedded designs secure? Do you worry about your next product being vulnerable to attacks by hackers? This webcast will look at how the royalty-free INTEGRITY real-time operating system takes advantage of the Blackfin architecture, including the Memory Protection Unit, allowing you to build totally reliable, absolutely secure, and maximum performance products—in the least time and with the lowest production cost. ■

JUNE
29

Performance Clocks: Demystifying Jitter

2:00 pm ET/11:00 am PT — Analog Devices, Inc.

Join us as we delve into the realm of sub-picosecond jitter clocks. The relationship between jitter and phase noise will be explored in detail and methods for measuring sub-picosecond jitter and ultra low phase noise will be discussed. This NetSeminar will cover performance clock IC applications and considerations and the use of ADI's new ADI SimCLOCK clock simulation tool will be featured. ■

View these recently archived NetSeminars anytime:

- Introducing the AMCC PowerPC 440EPx and 440GRx Security-Enabled Processors — AMCC Corp.
- TTI Technical Seminar Series: Be Smart - Choose the Right Parts Capacitors: Choose the Right Cap for the Right App! — TTI, Inc.
- Cypress 2.4GHz Wireless Solutions — One Stop Shop Cypress Semiconductor
- Leveraging Advanced Converter Architectures for Impedance and Capacitance Sensors — Analog Devices, Inc.
- Simplified Field System Upgrades with Instant-On, Flash FPGAs — Lattice Semiconductor

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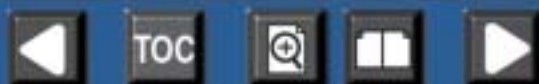


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IBM timing tool

FROM PAGE 1

EinsTimer has been IBM's gate-level static timer for more than a decade. The tool's statistical capability has been in use at IBM for about a year, and the company has been phasing statistical methods into design kits over the past three years.

Can IBM translate that into commercial EDA success? The company in the past has fielded such EDA technologies as timing analysis, test and, most recently, formal verification, but it has never amassed much market share in the design tool market.

"If IBM really wants to succeed as an EDA vendor, they can," said Gary Smith, chief EDA analyst at Gartner Dataquest. But the industry giant's past attempts at commercializing EDA technology have been "half-hearted," he said.

Smith called EinsTimer's statistical capability "state of the art" and said statistical timing will be needed by IC layout teams at 45 and 65 nanometers. "They picked a good tool this time," he said. The open questions are whether it can be used by non-IBM engineers and whether IBM will adequately market and support it.

The latter is the domain of IBM's ET&S division, which was founded in 2002 and today employs 1,300 engineers. "A software-licensing solution is complementary to our services offering," said Hoffman. But "we don't think users want point tools; they want solutions," he said. "Software licensing is just one component of what we offer."

The EinsTimer suite includes gate- and transistor-level static timing analysis, statistical timing analysis, power distribution analysis and signal integrity. It comes

with a characterization tool that can work with data from commercial foundries.

Startup Extreme DA claims to be close on IBM's heels. CEO Mustafa Celik said his company's statistical timing tool has reached production quality and will probably be announced in July. The offering will include a statistical extractor and a library characterization tool, with signal integrity soon to follow. Celik said that his

ed. While layout engineers need it at 65 nm, design engineers won't need it until 45 nm or below, said Dataquest's Smith.

"We expect to see statistical timing methods appearing in 2006 for very high-end-performance designs at 65 nm," said Eric Filseth, vice president of marketing for digital implementation at Cadence Design Systems Inc. "A huge amount of silicon infrastructure and supply chain

needed for quite a while," said Chandu Visweswariah, manager of circuit and interconnect analysis at IBM Research. "Analog designs have used statistical methods for years."

Visweswariah said EinsTimer can handle front-end variations like L-effective, hot electron effect and different voltage thresholds; back-end variations such as metal separation and width; and environmental variations like temperature and V_{dd} .

What most distinguishes statistical timing analysis is the outputs it produces. They may include probability distributions for slack margins, sensitivity reports that link timing and process variables, predictions of worst-case performance across the performance space, and yield curves for different frequencies.

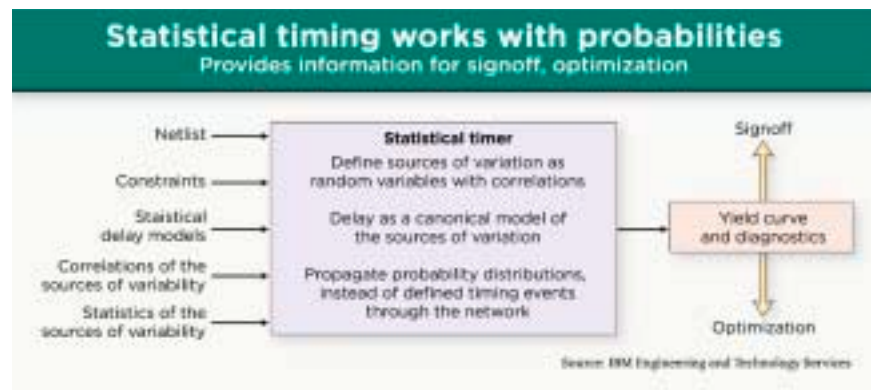
New mind-set

The problem is the input. Statistical timers need to know the sensitivity of the delay of library elements to each process variable. EinsTimer comes with characterization software that can extract that information from foundry-supplied libraries, Visweswariah said.

Visweswariah acknowledged that statistical timing requires a new way of thinking, since what used to be one number now becomes a probability distribution. But he said there are ways of easing into statistical analysis, such as asking for a Three Sigma report on slack distribution.

Although the statistical capability is built on top of the EinsTimer static timing analyzer, designers can continue to sign off with other static timing analyzers, such as Synopsys' market-leading PrimeTime, Visweswariah said.

Although the suite is available now, IBM declined to discuss pricing.



seven-person startup is not worried about competition from EinsTimer, which he views more as a "point tool" used inside IBM than as a full statistical environment.

Magma's Quartz SSTA statistical timing analyzer, which includes extraction and library characterization, is in alpha release with early customers, and production release is expected later in the year, said Suk Lee, general manager of Magma's silicon signoff business unit. "IBM cannot offer an integrated, competitive solution," Lee said. "Because it's targeted for IBM's flow, IBM will have difficulty commercializing EinsTimer."

Meanwhile, there are questions about how soon statistical timing will be need-

work needs to be done in the meantime."

Statistical timing analysis will initially target 65 nm and see mainstream use at 45 nm, said Rajiv Maheshwary, senior director of marketing for signoff and power products at Synopsys Inc. He said Synopsys is "partnering closely with customers" on variation-aware analysis and extraction.

Statistical analysis is of interest because nanometer IC designs are subject to high process variability. Designers can control variability by applying guardbands, but they will give up performance to do so, statistical timing advocates say. Statistical tools can examine all the possible corner conditions created by process variations.

"Statistical timing is something we've

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Cell phone SoCs

FROM PAGE 1

phones. Multi-megapixel imaging capability may seem moot when most mobile operators today acknowledge that few subscribers ever upload their snapshots off their phones. But as Nethra's president and CEO, Singh is convinced of the potential mass appeal of dedicated image processing and says Nethra's SoCs will convincingly make the point that "megapixel [alone] doesn't necessarily translate into better image quality."

Nethra's engine processes raw data captured by a CMOS or CCD 3-Mpixel image processor to yield an image that the company says is comparable in quality to a high-end digital still camera image. The SoC's enhanced processing yields truer color reproduction and captures image details that elude lower-quality processing engines, the company says.

Tony Henning, managing editor of Future Image Inc.'s Mobile Imaging Report, acknowledged that "a dedicated image processor with clever algorithms—and the processing power and memory necessary to execute them properly—can have a dramatic impact on the quality of a digital image, especially if the algorithms operate on the raw data before it's been abused by poor processing or aggressive compression."

Henning sees a market for such technology if three conditions are met: customers demand better phone photos, operators see an opportunity for brand recognition based on imaging, and prices for quality imaging components approach parity with what's available today in the United States.

Allen Noguee, principal analyst at In-Stat, sees "lots of value add" in image processing, especially in camera phones.

But with the KISS strategy finding increasing favor with mobile operators, some aren't buying Nethra's assumption of a 3-Mpixel sweet spot for camera phones by next year.

"People will realize very quickly that what they really want is a 1- or 2-Mpixel camera, because that's good enough," David Hytha, executive vice president of T-Mobile, recently told *EE Times*. "Some people will work on improving quality through software and maybe a little hardware, maybe a little bit of work on the lenses. But if somebody thinks that 3-megapixel is a mass market, I wish him luck."

Singh doesn't think he'll need it, if Nethra does its job. "The message of 'print quality' has to get out," he said. Consumers aren't uploading images, he said, because "the quality isn't there," and high-speed data services are still in development.

Track record

Nethra (Cupertino, Calif.), incorporated in 2003, is no stranger to the business. Singh earlier founded MediaQ, a developer of graphics and imaging ASICs for wireless handsets that was acquired by Nvidia Corp. in 2003. Murty Bhavana, Nethra co-founder and vice president of

marketing, also worked at MediaQ and, before that, at NuCore Technology, a developer of imaging ASICs for consumer digital still cameras and digital camcorders.

"MediaQ helped us understand operators, cell phone [makers] and the shift in the handset market," said Singh. The latest requests for proposals from handset vendors, he said, include 720 x 480 D1 resolution images at 30 frames/second, with full TV-type video capture resolution.

Rather than build its imaging processor into a sensor or an application/baseband processor, Nethra developed a programmable SoC that it claims outperforms its competitors' DSPs and ASICs in handling multi-megapixel imaging. Because 2- or 3-Mpixel sensors require compute-intensive image processing, the company said, the SoC architecture was built to support the needs of the core pipeline. Thus, handset memory bandwidth does not become a bottleneck.

Along with the image-processing engine, Nethra's SoC integrates 32 kbytes of SRAM, 64 kbytes of embedded flash, an ARM7 core and a synchronous DRAM in an 8-mm-square chip-scale package with a 1.0- to 1.2-mm mounted profile.

The on-chip ARM 7 core runs proprietary camera algorithms for such elements as automatic exposure, auto white balance, autofocus and red-eye correction. Other advanced features, such as adaptive light control, enhanced night mode and electronic image stabilization, are hardware-enabled in the SoC's image-processing engine.

The embedded flash contains the software to tune the picture quality and enable system control. Camera applications communicate with the camera via I²C. Color-tuning parameters for a range of commercial sensors are embedded in the flash.

The platform also works with various application processors and, thus, is "adaptable to multiple end products," said Bhavana.

Nethra's Ni-20x0 development platform is available now, and chips are sampling to selected customers. The chips, fabricated in a 0.18-micron process at Taiwan Semiconductor Manufacturing Co. Ltd., are slated for volume production in the third quarter. NI-2060, the base product in a chip-scale package, is priced at \$8 in volumes of 10,000. The NI-2080, offering advanced features with 8 Mbytes of stacked internal SDRAM, is priced at \$12.

Nethra believes it will take at least 12 to 15 months for competitors such as Nvidia and ATI Technologies to catch up with the startup's SoC. Bhavana added that it may take even longer—18 to 24 months—for

application/baseband processor vendors such as Texas Instruments and Qualcomm to integrate comparable features at lower power levels.

The window of opportunity for Nethra to succeed, however, may be closing fast, as the integration of chips and functions accelerates.

Nethra claims relationships with top handset vendors, including Nokia, Samsung, Motorola and Sony-Ericsson, and its executives say they're confident in the growing need for independent image processors that let OEMs choose either a CCD or a CMOS sensor.

"Handset vendors don't

Key managers at Nethra

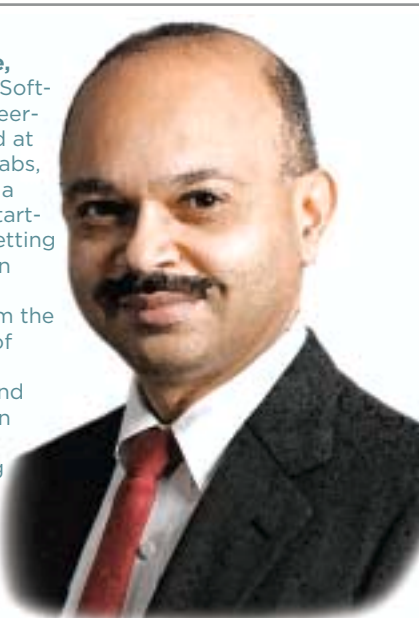
Dr. Ping Wah Wong, Vice President, Chief Imaging Scientist: Previously, Ping managed a research team at Hewlett Packard Laboratories. He is current and past associate editor for the Journal of Electronic Imaging and IEEE Transaction on Image Processing.



Ravi Bhatnagar, Senior VP, Engineering, Co-Founder: Former VP of business development at NeoMagic, which he joined when it bought Link Up Systems Inc., a company he founded. Before that he held positions at Chips & Technologies and Cirrus Logic.



Srini Amble, Director of Software Engineering: Worked at AT&T Bell Labs, Fujitsu and a couple of startups after getting a master's in computer science from the University of Texas at Arlington and a master's in mechanical engineering from University of Akron, Ohio.



like to depend on a single country—Japan—to source their CCD sensors from," said Singh. Nethra's sensor-agnostic imaging processor, he said, can help the CMOS sensor "keep its edge."

Future Image's Henning predicted the industry will start to see 3-megapixel camera phones in the United States by the end of this year. The phones' market share in 2006 will not exceed 10 percent of the global camera-phone market, he said, but 3-megapixel-and-higher camera phones will dominate the market, with more than a 50 percent share, by 2009.

Ramesh Singh, President, CEO, Co-Founder: Former sales vp at NVidia who joined that company when it acquired MediaQ Inc., a company he founded. Before that, Singh ran the Home Products Division at S3 Inc.





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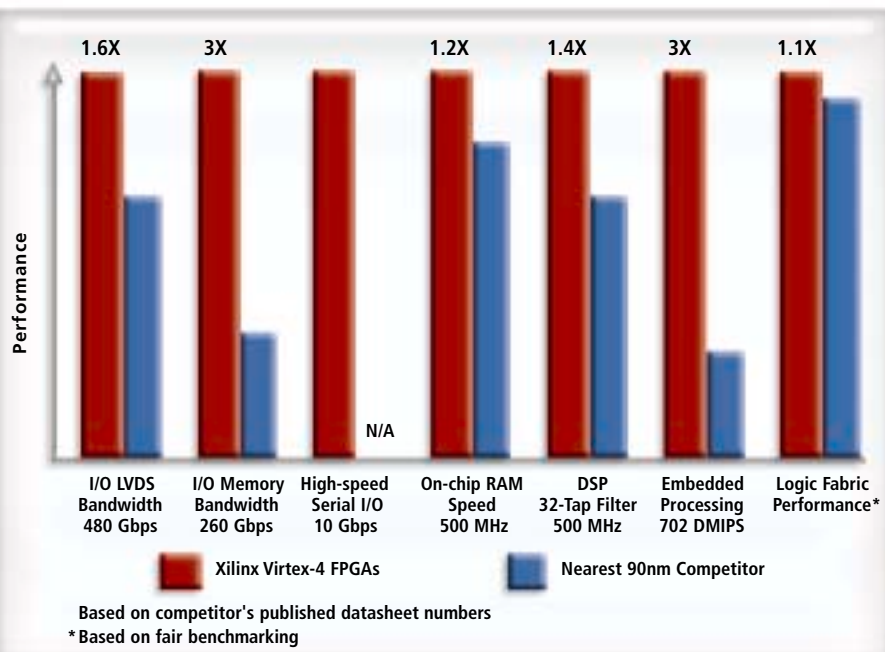
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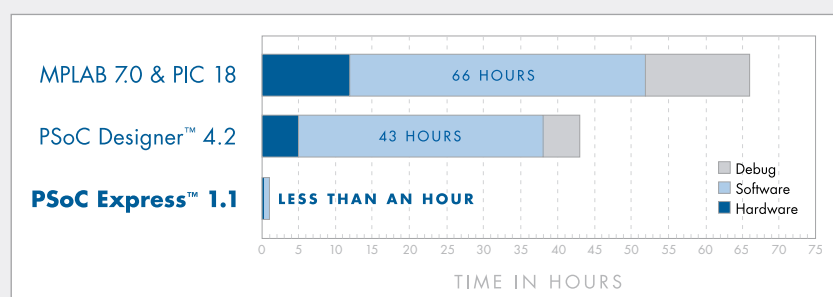
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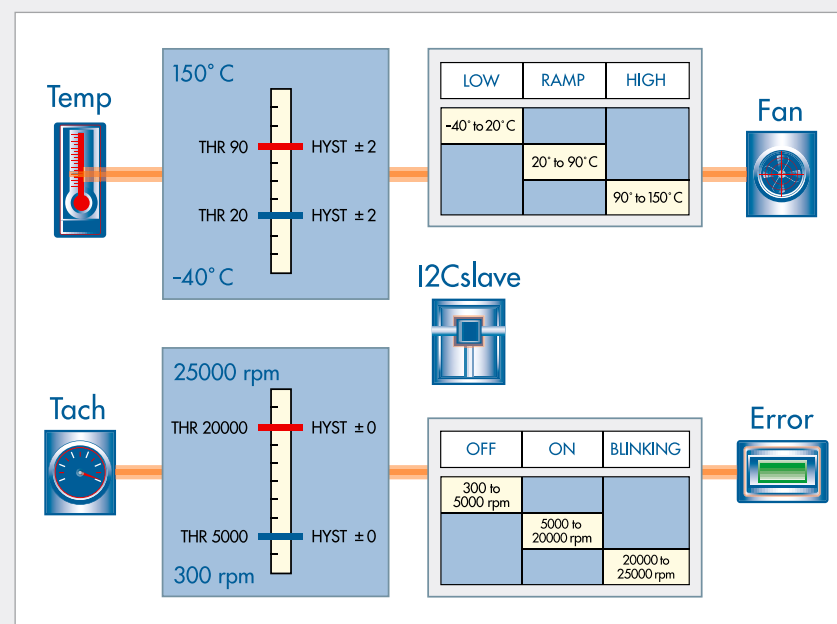
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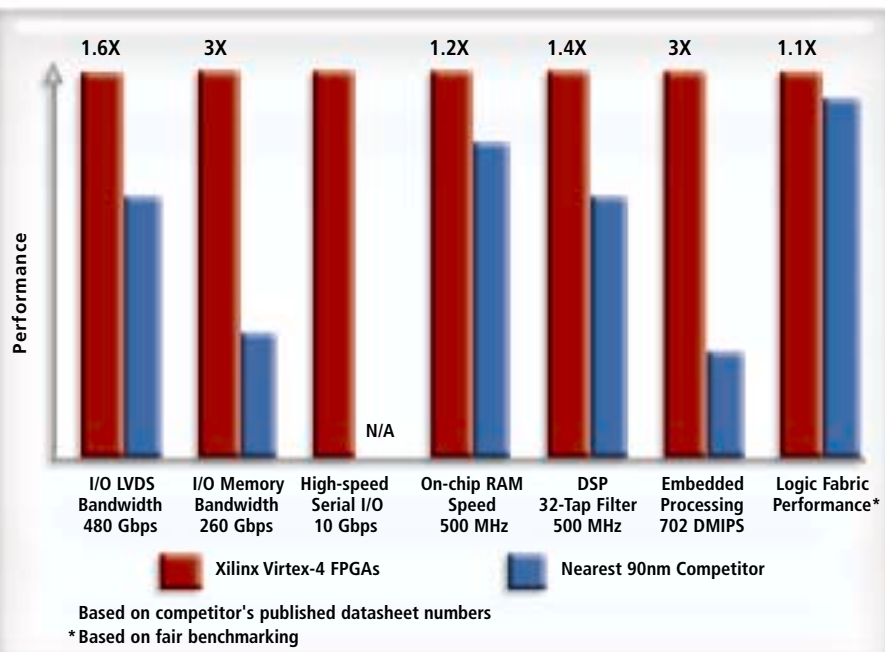
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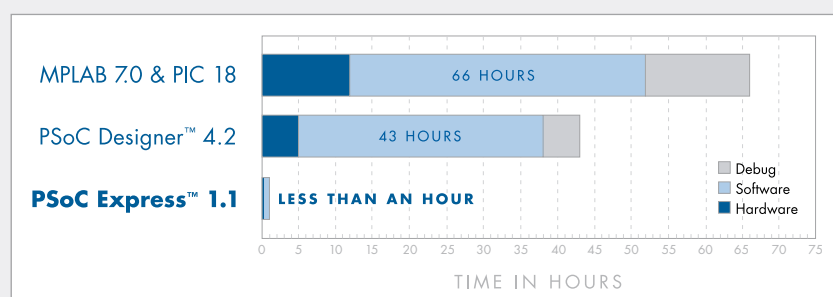
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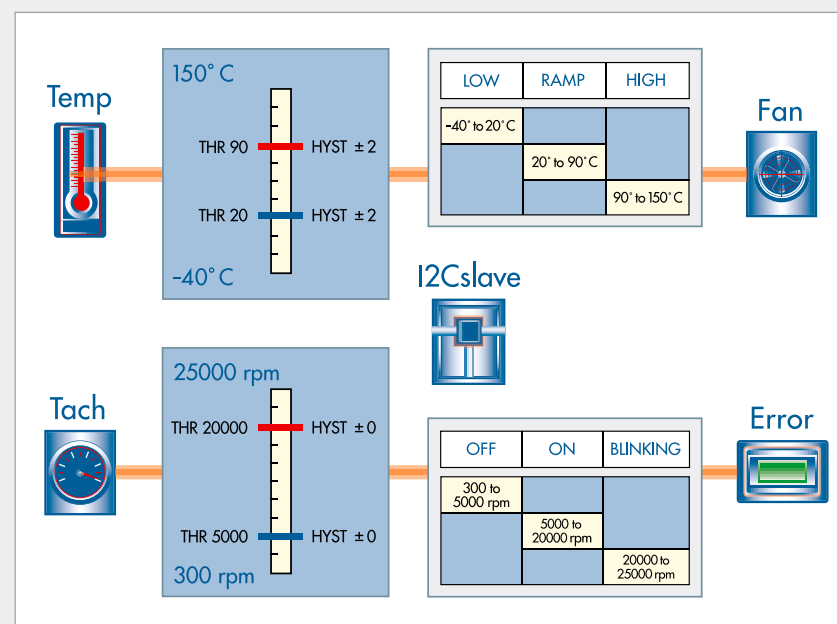
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